MC-12 / MC-12 Balanced

Music and Cinema Processors

Service Manual

Lexicon

Precautions
Save these instructions for later use.

Follow all instructions and warnings marked on the unit.

Always use with the correct line voltage. Refer to the manufacturer's operating instructions for power requirements. Be advised that different operating voltages may require the use of a different line cord and/or attachment plug.

Do not install the unit in an unventilated rack, or directly above heat producing equipment such as power amplifiers. Observe the maximum ambient operating temperature listed in the product specification.

Slots and openings on the case are provided for ventilation; to ensure reliable operation and prevent it from overheating, these openings must not be blocked or covered. Never push objects of any kind through any of the ventilation slots. Never spill a liquid of any kind on the unit.

This product is equipped with a 3-wire grounding type plug. This is a safety feature and should not be defeated.

Never attach audio power amplifier outputs directly to any of the unit’s connectors.

To prevent shock or fire hazard, do not expose the unit to rain or moisture, or operate it where it will be exposed to water.

Do not attempt to operate the unit if it has been dropped, damaged, exposed to liquids, or if it exhibits a distinct change in performance indicating the need for service.

This unit should only be opened by qualified service personnel. Removing covers will expose you to hazardous voltages.

This triangle, which appears on your component, alerts you to the presence of uninsulated, dangerous voltage inside the enclosure… voltage that may be sufficient to constitute a risk of shock.

CAUTION

RISK OF ELECTRIC SHOCK
DO NOT OPEN

This triangle, which appears on your component, alerts you to important operating and maintenance Instructions in this accompanying literature.

Notice
This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications of Part 15 of FCC Rules, which are designated to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment OFF and ON, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna
- Relocate the computer with respect to the receiver
- Move the computer away from the receiver
- Plug the computer into a different outlet so that the computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

“How to identify and Resolve Radio/TV Interference Problems"

This booklet is available from the U.S. Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class B prescrites dans le Règlement sur le brouillage radioélectrique édicté par le ministère des Communications du Canada.

Lexicon Inc. ● 3 Oak Park ● Bedford, MA 01730-1441 ● Tel (781) 280-0300 ● Customer Service Fax (781) 280-0499
Lexicon Part # 070-14828 Rev 0
Printed in the United States of America

Safety Suggestions

Read Instructions Read all safety and operating instructions before operating the unit.

Retain Instructions Keep the safety and operating instructions for future reference.

Heed Warnings Adhere to all warnings on the unit and in the operating instructions.

Follow Instructions Follow operating and use instructions.

Heat Keep the unit away from heat sources such as radiators, heat registers, stoves, etc., including amplifiers which produce heat.

Ventilation Make sure that the location or position of the unit does not interfere with its proper ventilation. For example, the unit should not be situated on a bed, sofa, rug, or similar surface that may block the ventilation openings; or, placed in a cabinet which impedes the flow of air through the ventilation openings.

Wall or Ceiling Mounting Do not mount the unit to a wall or ceiling except as recommended by the manufacturer.

Power Sources Connect the unit only to a power supply of the type described in the operating instructions, or as marked on the unit.

Grounding or Polarization* Take precautions not to defeat the grounding or polarization of the unit's power cord.
*Not applicable in Canada.

Power Cord Protection Route power supply cords so that they are not likely to be walked on or pinched by items placed on or against them, paying particular attention to cords at plugs, convenience receptacles, and the point at which they exit from the unit.

Nonuse Periods Unplug the power cord of the unit from the outlet when the unit is to be left unused for a long period of time.

Water and Moisture Do not use the unit near water — for example, near a sink, in a wet basement, near a swimming pool, near an open window, etc.

Object and Liquid Entry Do not allow objects to fall or liquids to be spilled into the enclosure through openings.

Cleaning The unit should be cleaned only as recommended by the manufacturer.

Servicing Do not attempt any service beyond that described in the operating instructions. Refer all other service needs to qualified service personnel.

Damage Requiring Service The unit should be serviced by qualified service personnel when: the power supply cord or the plug has been damaged; objects have fallen or liquid has been spilled into the unit; the unit has been exposed to rain; the unit does not appear to operate normally or exhibits a marked change in performance; the unit has been dropped, or the enclosure damaged.

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in these instructions violates safety standards of design manufacture and intended use of the instrument. Lexicon assumes no liability for the customer's failure to comply with these requirements**.**

GROUND THE INSTRUMENT

To minimize shock hazard the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor AC power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

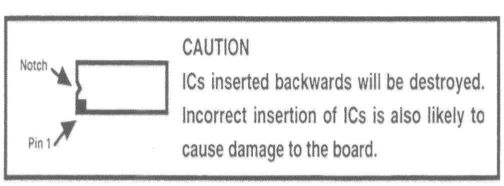
Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

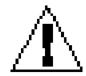
WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing and adjusting.

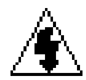


SAFETY SYMBOLS

General definitions of safety symbols used on equipment or in manuals.



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.



Indicates dangerous voltage. (Terminals fed from the interior by voltage exceeding 1000 volts must be so marked.)

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

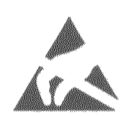
NOTE:

The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like which is essential to highlight.

CAUTION

Electrostatic Discharge (ESD) Precautions

The following practices minimize possible damage to ICs resulting from electrostatic discharge or improper insertion.



- Keep parts in original containers until ready for use.
- Avoid having plastic, vinyl or styrofoam in the work area.
- Wear an anti—static wrist-strap.
- Discharge personal static before handling devices.
- Remove and insert boards with care.
- When removing boards, handle only by non-conductive surfaces and never touch open-edge connectors except at a static-free workstation.*
- Minimize handling of ICs.
- Handle each IC by its body.
- Do not slide ICs or boards over any surface.
- Insert ICs with the proper orientation, and watch for bent pins on ICs.
- Use static shielding containers for handling and transport.

'To make a plastic-laminated workbench anti-static, wash with a solution of Lux liquid detergent, and allow drying without rinsing.

Table of Contents

Chapter 1 Reference Documents, Required Equipment

Reference Documents

MC-12/MC-12 Balanced User Guide - Lexicon P/N 070-14773, latest revision

Required Equipment

TOOLS

The following is a minimum suggested technician's tool kit required for performing disassembly, assembly and repairs:

- Clean, antistatic, well-lit work area with grounding wrist strap
- (1) #1 Phillips tip screwdriver - (Magnetic tip preferred)
- (1) 14mm socket nut driver
- (1) Allen hex head wrench (2.5 mm)
- (1) 3/16 hollow nutdriver
- Solder: 63/37 - Tin/Lead Alloy composition, low residue, no-clean solder
- Magnification glasses and lamps
- SMT Soldering/Desoldering bench-top repair station

TEST EQUIPMENT

The following is a *minimum* suggested equipment list required to perform the proof of performance tests.

- (1) High quality Amplifier with RCA and XLR input connectors
- (1) Pair high quality Speakers with RCA and XLR input connectors
- (1) High quality Video Monitor with RCA, S-Video, and Component (RCA and BNC) input connections
- (1) CD disc for test audio source
- (1) DVD movie disc for test video source
- Cables: (dependent on your signal source)
    - Audio Input Cables with shield and an RCA connector on one end and an appropriate connector on the opposite end for connection to the Low Distortion Oscillator
    - Audio Output Cable with shield and an RCA connector on one end and an appropriate connector on the opposite end for connection to the Distortion Analyzer
    - Audio Output Cable (balanced) with shield and an XLR female plug on one end and an appropriate connector on the opposite end for connection to the Distortion Analyzer
  - (4) Audio Cables shielded with RCA connectors on both ends
  - (2) Audio Cables shielded with an XLR male and female connector on either end
  - (1) Digital Audio Cable with RCA connectors on both ends
  - (1) Digital Audio Cable with Optical connectors on both ends
  - (1) AES/EBU Digital cable
  - (1) Digital Audio Cable with Standard Optical connector on one end and an OMJ (Optical Mini Jack) connector on the other
  - (2) Video Cables with RCA connectors on both ends
  - (2) Video Cables with S-Video connectors on both ends
  - (1) Video Cable with 3-wire Component RCA connectors on both ends
  - (2) Video Cables with 3-wire Component BNC connectors on both ends
  - (1) High end DVD player with RCA Analog Left and Right and Digital Coax and Optical Audio Outputs
  - (1) MC-12 AC power cord
- variable AC power supply 2 amp minimum
- Digital Multimeter (DMM) 3.5 digit 0.5% or better accuracy

- (1) Low Distortion Analog oscillator with single-ended or balanced output, < 100 ohms output impedance, < .005% THD
- (1) Analog Distortion Analyzer and Level Meter with single-ended or balanced input, switchable 30Hz high pass filter or audio bandpass (20-20kHz) filter
- (1) 100 MHz Oscilloscope
- (1) Digital Distortion Analyzer & Digital Function Generator (e.g. Stanford Research Systems Model DS360 or Audio Precision System 1 with DSP Option/System 2).

Chapter 2 General Information

Periodic Maintenance

Under normal conditions the MC-12/MC-12 Balanced requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and mild detergent to clean the exterior surfaces of the connector box.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners. DO NOT use abrasive materials such as steel wool or metal polish. If the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the unit's exterior.

Ordering Parts

When ordering parts, identify each part by type, price and Lexicon Part Number. Replacement parts can be ordered from:

LEXICON, INC.
3 Oak Park
Bedford, MA 01730-1441
Telephone: 781-280-0300; Fax: 781-280-0499; email: csupport@lexicon.com
ATTN: Customer Service

Returning Units to Lexicon for Service

Before returning a unit for warranty or non-warranty service, consult with Lexicon Customer Service to determine the extent of the problem and to obtain Return Authorization. No equipment will be accepted without Return Authorization from Lexicon.

If Lexicon recommends that an MC-12/MC-12 Balanced should be returned for repair and you choose to return the unit to Lexicon for service, Lexicon assumes no responsibility for the unit in shipment from the customer to the factory, whether the unit is in or out of warranty. All shipments must be well-packed (using the original packing materials if possible), properly insured and consigned, prepaid, to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Your Name
- Company Name
- Street Address
- City, State, Zip Code, Country
- Telephone number (including area code and country code where applicable)
- Serial Number of the unit
- Description of the problem
- Preferred method of return shipment
- Return Authorization #, on both the inside and outside of the package

Please enclose a brief note describing any conversations with Lexicon personnel (indicate the name of the person at Lexicon) and give the name and daytime telephone number of the person directly responsible for maintaining the unit.

Do not include accessories such as manuals, audio cables, footswitches, etc. with the unit, unless specifically requested to do so by Lexicon Customer Service personnel.

Chapter 3 Specifications

Audio Inputs and Outputs

Audio Inputs - 8 stereo pairs (RCA) *or* 5 stereo pairs and one 5.1-channel analog input
Digital Audio Inputs - 6 coaxial (RCA), 6 optical (5 TosLink, and 1 optical mini jack), 1 AES/EBU; coaxial and optical inputs conform to IEC-958, S/PDIF standards
Sample Rates: 44.1, 48, 88.2, 96kHz
Accepts: 16-24 bits PCM audio, Dolby Digital, dts and dts-ES discrete data formats
Main Audio Outputs - 12 unbalanced (RCA) and 12 balanced (XLR, MC-12 Balanced only) for Front L/R, Center, LFE, Subwoofer L/R, Side L/R, Rear L/R, Auxiliary L/R
Zone 2 Audio Outputs - 2 stereo pairs (RCA, one fixed and one variable output level); 2 balanced (XLR) for L/R variable output (MC-12 Balanced only)
Record Audio Outputs - 2 stereo pairs (RCA, one fixed and one variable output level); 1 coaxial (RCA) and 1 optical (TosLink) S/PDIF output (in parallel)

Performance (Main Zone)

Analog-to-Digital Conversion - 24-bit, 96kHz, dual-bit ΔΣ architecture
Digital-to-Analog Conversion - 24-bit, 44.1 to 192kHz, multi-bit ΔΣ architecture, operating in dual-mono mode
Frequency Response - 10Hz to 20kHz, +0.1dB/-0.25dB, -0.75dB at 40 kHz, reference 1kHz
THD + Noise - Below 0.003% at 1kHz, maximum output level
Dynamic Range - 108dB minimum, 111dB typical, 22kHz bandwidth
Signal-to-Noise Ratio - 108dB minimum, 111dB typical, 22kHz bandwidth
Input Sensitivity - 200mVrms (2Vrms for maximum output level) at 0dB input gain
Input Impedance - 100kΩ in parallel with 150pF
Output Level - 150mVrms typical, 6Vrms maximum (RCA outputs); 300mVrms typ, 12Vrms maximum (XLR outputs, MC-12 Balanced only); maximum value with full-scale input signal and volume at +12dB
Output Impedance - 100Ω in parallel with 150pF (RCA outputs); 50Ω in parallel with 150pF (XLR outputs, MC-12 Balanced only)

Performance (Zone 2 and Record Zone)

Analog-to-Digital Conversion - 24-bit, 44.1 to 96kHz, dual-bit ΔΣ architecture (Record Zone only)
Digital-to-Analog Conversion - 24-bit, 44.1 to 192kHz, multi-bit ΔΣ architecture
Frequency Response - 10Hz to 20kHz, +0.1dB/-0.25dB, -0.75dB at 40kHz, reference 1kHz
THD + Noise Below 0.005% at 1kHz, maximum output level
Dynamic Range - 105dB minimum, 108dB typical, 22kHz bandwidth
Signal-to-Noise Ratio - 105dB minimum, 108dB typical, 22kHz bandwidth
Input Sensitivity - 200mVrms (4Vrms for maximum output level)
Input Impedance - 100 kΩ in parallel with 150pF
Output Level - 200mVrms typical, 4Vrms maximum (RCA outputs); 400mVrms typical, 8Vrms maximum (XLR outputs, Zone 2 only, MC-12 Balanced only); maximum value with full-scale input signal and volume at 0dB
Output Impedance - 100Ω in parallel with 150pF (RCA outputs); 50Ω in parallel with 150pF (XLR outputs, Zone 2 only, MC-12 Balanced only)

Video Inputs and Outputs

Video Inputs - 5 composite (RCA), 8 S-video, and 4 component video (3 RCA, 1 BNC)
Video Outputs - 4 composite (RCA, 2 monitor and 2 record), 4 S-video (2 monitor and 2 record), and 1 component (BNC)

Performance (Composite & S-video)

NTSC M, PAL, and SECAM compatible
Switching - Active
Output Level - 1.0V peak-to-peak
Impedance - 75Ω
Input Return Loss - >40dB
Differential Gain - <0.5%
Differential Phase - <0.5°
Bandwidth - >25MHz
K Factor - <0.3%

Gain - ±0.15dB
Signal/Noise Ratio - >70dB
Frequency Response - 10Hz to 10MHz + 0.1/-0.3dB

Performance (Component Video)

3-channel (Y, Pr, Pb), format-independent
Switching - Passive
Impedance - 75Ω
Bandwidth - >300MHz
Insertion Loss - <3dB

Other

Microphone Inputs - 4 3.5mm miniature phone jacks
  Input sensitivity: 10mVrms (400mV maximum input level)
  Input Impedance: 20kΩ (accepts balanced or unbalanced input signals)
Trigger Outputs - 1 power-on/off trigger, 2 programmable triggers; +12 VDC, 0.5 amps each; detachable screw terminals
RS-232 Serial Input/Output - 2 9-pin D-sub connectors for system control and software upgrades
Power Requirements - 90-250 VAC, 50-60Hz, 90W (universal line input), detachable power cord
Dimensions -
  MC-12: 17.3"w x 5.2"h x 14.85"d (440 x 132 x 377mm)
  MC-12 Balanced: 17.3"w x 6.63"h x 14.85"d (440 x 169 x 377mm)
Weight -
  MC-12: 36lbs (16.4kg)
  MC-12 Balanced: 45lbs (20.5kg)
Rack Mounting - Optional brackets are available for mounting either unit in a standard 19" equipment rack
Environment
  Operating Temp: 0° to 35°C (32° to 95°F)
  Storage Temp: -30° to 75°C (-22° to 167°F)
  Relative Humidity: 95% maximum without condensation
Remote Control - Hand-held, battery-powered infrared remote control unit
  Batteries: Two AA

Chapter 4 Perfo rmance Verification

This section describes a quick verification of the operation of the MC-12/MC-12 Balanced and the integrity of its analog and digital audio signal paths. Tests are included for the MC-12 Balanced version and can be omitted when testing an MC-12/MC-12 Balanced.

Functional Tests

The following tests cover basic functions making sure the MC-12/MC-12 Balanced responds to button commands from the remote as well as from its front panel.

INITIAL INSPECTION

1. Inspect the MC-12/MC-12 Balanced for obvious signs of physical damage.
2. Verify that all switches operate smoothly.
3. Remove the MC-12/MC-12 Balanced top cover.
4. Verify that all socketed ICs are correctly seated.
5. Verify that all ribbon cables are correctly installed and are secure.
6. Check for burnt or obviously damaged components.
7. Using the main power switch on the back of the MC-12/MC-12 Balanced, verify that it runs through its Diagnostics Test and settles into the last state it was powered down in.
8. Check each of the front panel's switches for smooth mechanical operation, that each LED turns on and off when depressed, and that the display acknowledges its function.
9. Press all the buttons on the remote and verify that the display is responding to all the remote commands.

POWER SUPPLY TEST

The main power supply in the MC-12/MC-12 Balanced has an operational range of 100-240 VAC 50-60Hz, 90Watts.
The following test is for North American line voltage of 120VAC.

1. Set the variable AC supply to 0 volts.
2. Verify that the MC-12/MC-12 Balanced is powered off at its rear panel power switch.
3. Connect the power cord between the supply and the MC-12/MC-12 Balanced.
4. Turn on the MC-12/MC-12 Balanced using the rear panel power switch.
5. Slowly bring up the voltage to 120VAC.
6. The current draw will bounce up and down a bit and should not exceed 1.5amps. Once you have achieved 120VAC the current draw on the Variac should not exceed 0.6amps. If the MC-12/MC-12 Balanced draws an excessive current, turn the MC-12/MC-12 Balanced off and check the power supply rails for shorts to ground with the DMM meter.
7. Using the DMM measure all the power supply rails as stated by the test points below, being sure to use the MC-12/MC-12 Balanced chassis as ground
8. Verify that all voltages are within the tolerance range shown.

Main Board

Supply Rail	Tolerance	Location (facing front panel)
+5VD	4.94-5.26	Lower left-hand corner connector J31 Red wires to ground.
Battery	≥ 2.5	Right side to the Left of U69; Measure the top of the battery to ground

Note: If battery is in need of replacement

CAUTION

"CAUTION Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type."

Analog Board

Supply Rail	Tolerance	Location (facing front panel)
+5VDC	4.75-5.25VDC	Lower left hand corner connector J26.Red wire to ground
-5VDC	4.75-5.25VDC	J26 Grey wire to ground
+15V	15.00-16.95	J26 Yellow wire to ground
-15V	14.25-15.75	J26 Blue wire to ground

Video Board

Supply Rail	Tolerance	Location (facing front panel)
+5VA	4.75-5.26	Lower left hand corner connector J22. Red wire to ground
-5VA	4.75-5.26	J22 Grey wire to ground

SETUP

In order to properly test the MC-12/MC-12 Balanced as described in this document, follow this setup procedure before hand. It will make it much easier to follow along and perform each of the tests to follow.

1. Connect a small color monitor to the Composite output. This will allow you to fully view the diagnostic menus of the MC-12/MC-12 Balanced.
2. Press and hold down the Zone 2 LD and the Record LD buttons on the front panel while powering up the MC-12/MC-12 Balanced with the Main Power Switch on the back of the unit.
3. Once the display reads Lexicon, release the buttons on the front panel.
4. The Display on the front panel will read DIAGS MENU FUNCTIONAL TESTS and the monitor will have a distorted, fractured-looking screen. This will happen on the monitor every time Diagnostics are loaded.
5. To clear this display, press the Down Menu button (or turn the Volume knob) on the remote until you see 'VIDEO I/O TESTS' displayed on their front panel.
6. Press the Right Menu Button (or the Mode button on the front panel) to enter the top of the VIDEO I/O TESTS Menu.
7. Press the Down button (or Modes Down button on the front panel) several times until you see 'LOAD FONT' displayed on the front panel.
8. Press Right Menu button (or Modes Down button on the front panel) to load the Fonts. The Monitor will turn to a blue screen and the front panel will read VIDEO I/O TESTS completed.
9. Press the Left Menu button (or the Mode Up button on the front panel) to bring a clear legible menu to the monitor screen. The monitor will display the VIDEO I/O TESTS menu with LOAD FONT highlighted with a black bar.
10. Press the Left Menu button (or Mode Up button on the front panel) to bring you to the main DIAGS MENU. The MC-12/MC-12 Balanced is now set up for monitor display for easier navigation through the Diagnostic menus.

Note: The tests to follow assume you have entered the Diagnostics Menu as described above. Each test will not repeat this setup procedure. It will make reference to it in order to set the stage for proper testing of the MC-12/MC-12 Balanced.

AUDIO TESTS I/O

Analog Input To ALL Analog Outputs Test

In this test we will be verifying the path of the #1 Left and Right RCA paired input to all Analog Outputs both RCA and XLR of the MC-12/MC-12 Balanced.

1. Connect the oscillator output to the Left and Right audio inputs marked #1 on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Front outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs, and the outputs of the amplifier to a pair of speakers.

3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight Audio Input 1 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set for audio coming into the Left and Right #1 RCA input to the Front Left and Right RCA output and all the remaining RCA and XLR paired Left and Right audio output connections.
6. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
7. Sweep the oscillator from 20Hz to 20kHz. Verify that you hear clean, clear audio coming from the speakers.
8. Power down the amplifier and move the cables from the Front Left and Right outputs to the Center Left and Right outputs.
9. Power on the amplifier and repeat the oscillator sweep as described in Step 7.
10. Repeat steps 8 and 9 for the remaining paired RCA outputs up to the Left and Right Aux. The Zone 2 and Record outs will be tested later.
11. To test the XLR paired outputs, power down the amplifier and remove the RCA output cables from the MC-12/MC-12 Balanced to the amplifier.
12. Connect a pair of XLR cables. Connect the Front Left and Right balanced outputs of the MC-12/MC-12 Balanced to the XLR balanced input of the amplifier.
13. Repeat step 7.
14. Test the remaining XLR Left and Right balanced outputs and Center L/R to AUX L/R by powering down the amp and repeating step 9.

All Remaining Analog Inputs to Analog Output Test

This test will verify the path of the remaining analog Left and Right inputs #2 to 8 to the Main Front Left and Right analog outputs pass signal.

1. Connect the oscillator output to the Left and Right audio inputs marked #2 on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Front outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs, and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight Audio Input 2 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set for audio coming in to the Left and Right #2 RCA input and out to the Front Left and Right RCA output.
6. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
7. Sweep the oscillator from 20Hz to 20kHz. Verify that you hear clean, clear audio coming from the speakers.
8. In order to test the remaining Analog inputs you must power down the amplifier and move the input cables to the next paired audio inputs.
9. Repeat steps 4 & 5 above highlighting the next input to be tested in the Audio I/O Tests Menu and select it by pressing the Right Menu button.
10. Repeat steps 5 to 7 until all the Audio Inputs have been tested.

Analog Input to Zone 2 Output Test

This test will verify the path of the #1 Left and Right RCA paired input to the Zone 2 Fix and Var outputs.

1. Connect the oscillator output to the Left and Right audio inputs marked #1 on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Zone 2 Fix outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs, and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.

5. Highlight Audio Input 1 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set for audio coming in to the Left and Right #1 RCA input to the ZONE 2 Left and Right RCA outputs.
6. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
7. Sweep the oscillator from 20Hz to 20kHz. Verify that you hear clean, clear audio coming from the speakers.
8. Power down the amplifier and move the cables from the Zone 2 Fix Left and Right outputs to the Zone 2 Var Left and Right outputs.
9. Power on the amplifier and repeat the oscillator sweep as described in Step 7.
10. Remove the RCA output cables from the Zone 2 Var Left and Right outputs of the MC-12/MC-12 Balanced to the amplifier.
11. Connect a pair of XLR cables to the Left and Right Zone 2 Fix balanced outputs of the MC-12/MC-12 Balanced to the XLR balanced input of the amplifier.
12. Repeat steps 7 to 9.

All Remaining Analog Inputs to the ZONE 2 Fix Output Test

This test will verify the path of the remaining analog Left and Right inputs #2 to #8 to the Fix Zone 2 Left and Right analog outputs pass signal.

1. Connect the oscillator output to the Left and Right audio inputs marked #2 on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Zone 2 Fix outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight Audio Input 2 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set for audio coming into the Left and Right #2 RCA input to the ZONE 2 Left and Right RCA outputs.
6. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
7. Sweep the oscillator from 20Hz to 20kHz. Verify that you hear clean, clear audio coming from the speakers.
8. In order to test the remaining Analog inputs to the Zone 2 Fix output, you must power down the amplifier and move the input cables to the next paired audio inputs. Next, highlight the input being tested in the Audio I/O Tests Menu and select it by pressing the Right Menu button.
9. Repeat steps 5 to 7 until all the Audio Inputs have been tested.

Analog Input to Record Output Test

This test will verify the path of the #1 Left and Right RCA paired input to the Record Fix and Var outputs.

1. Connect the oscillator output to the Left and Right audio inputs marked #1 on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Record Fix outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight Audio Input 1 Test then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set for audio coming in to the Left and Right #1 RCA input to the Record Fix Left and Right outputs.
6. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
7. Sweep the oscillator from 20Hz to 20kHz. Verify that you hear clean, clear audio coming from the speakers.
8. Power down the amplifier and move the cables from the Record Fix Left and Right outputs to the Record Var Left and Right outputs.
9. Power on the amplifier and repeat the oscillator sweep as described in Step 7.

All Remaining Analog Inputs to the Record Fix Output Test

This test will verify the path of the remaining analog Left and Right inputs #2 to #8 to the Fix Record Left and Right analog outputs pass signal.

1. Connect the oscillator output to the Left and Right audio inputs marked #2 on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Record Fix outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight Audio Input 2 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see audio coming in to the Left and Right #2 RCA input to the Record Fix Left and Right outputs.
6. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
7. Sweep the oscillator from 20Hz to 20kHz. Verify that you hear clean, clear audio coming from the speakers.
8. In order to test the remaining Analog inputs to the Record Fix output, you must power down the amplifier move the input cables to the next paired audio inputs. Next, highlight the input being tested in the Audio I/O Tests Menu and select it by pressing the Right Menu button.
9. Repeat steps 5 to 7 until all the Audio Inputs have been tested.

Digital Input to all Analog Outputs Test

This test will verify the path of the #1 Coax digital input to all of the Main analog outputs, both RCA and XLR of the MC-12/MC-12 Balanced.

Note: This test requires the use of a DVD player as a source. Therefore, the tests to follow will be run at the 44.1kHz sample rate. To properly test the full sample range of the MC-12/MC-12 Balanced, you will need to repeat all of the Digital tests with 48, 88.2, and 96kHz sample rate sources.

1. Connect the digital output source DVD Player to the #1 Coax digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Front outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight S/PDIF Input CX1 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio from the S/PDIF #1 digital input to the Front Left and Right RCA output and all the remaining RCA and XLR paired Left and Right audio output connections.
6. Press play on the DVD player.
7. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
8. Verify that you hear clean, clear audio coming from the speakers.
9. Pause the DVD and power down the amplifier.
10. Move the cables from the Front Left and Right outputs to the Center Left and Right outputs.
11. Power on the amplifier press play on the DVD player and repeat Steps 7 - 8.
12. Repeat steps 7 - 10 for the remaining paired RCA outputs up to the Left and Right Aux. The Zone 2 and Record outs will be tested later. Remove the RCA output cables from the MC-12/MC-12 Balanced to the amplifier.
13. With a pair of XLR cables, connect the Left and Right balanced outputs of the MC-12/MC-12 Balanced to the XLR balanced input of the amplifier.
14. Repeat steps 7 - 10 for the remaining paired XLR balanced outputs up to the Left and Right Aux. As in the RCA test above the Zone 2 XLR will be tested later.

All Remaining Digital Inputs to Analog Output Test

This test will verify the path of all the remaining Coax and Optical Digital inputs to the Main Front Left and Right analog output.

Note: In order to test the Optical #6, which is an OMJ (Optical Mini Jack) style connector, you will need an Optical to OMJ adapter in order to make the proper connection.

1. Connect the digital output source DVD player to the #2 Coax digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Front outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight S/PDIF Input CX2 Test then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio coming in to the S/PDIF #2 digital input to the Front Left and Right RCA output.
6. Press play on the DVD player.
7. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
8. Verify that you hear clean, clear audio coming from the speakers.
9. Pause the DVD and power down the amplifier.
10. In order to test the remaining Digital inputs both RCA and Optical you must move the Digital Input cable to the next Digital input (RCA or Optical), then highlight the input being tested in the Audio I/O Tests Menu and select it by pressing the Right Menu button.
11. Repeat steps 6 - 8 until all the remaining Digital Inputs have been tested.

Digital Input to Zone 2 Output Test

This test will verify the path of the #1 Coax Digital input to the Zone 2 Fix and Var Left and Right outputs.

1. Connect the digital output source DVD player to the #1 Coax digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Zone 2 Fix outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight S/PDIF Input CX1 Test then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio from the S/PDIF #1 digital input to the Front Left and Right RCA output and all the remaining RCA and XLR paired Left and Right audio output connections.
6. Press play on the DVD player.
7. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
8. Verify that you hear clean, clear audio coming from the speakers.
9. Pause the DVD and power down the amplifier.
10. Move the cables from the Zone 2 Fix Left and Right outputs to the Zone 2 Var Left and Right outputs.
11. Power on the amplifier press play on the DVD player and repeat step 7 - 8.
12. Pause the DVD and power down the amplifier.
13. Remove the RCA output cables from the Zone 2 Var Left and Right outs of the MC-12/MC-12 Balanced to the amplifier.
14. With a pair of XLR cables connect the Left and Right Zone 2 Fix balanced outputs of the MC-12/MC-12 Balanced to the XLR balanced input of the amplifier.
15. Power on the amplifier, press play on the DVD player, and repeat Step 7 - 9.

All Remaining Digital Inputs to Zone 2 Output Test

This test will verify the path of all the remaining Digital Coax and Optical Digital inputs to the Zone 2 Fix Front Left and Right analog output.

Note: In order to test the Optical #6, which is an OMJ (Optical Mini Jack) style connector, you will need an Optical to OMJ adapter in order to make the proper connection.

1. Connect the digital output source DVD player to the #2 Coax Digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Zone 2 Fix outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight S/PDIF Input CX2 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio from the S/PDIF #2 digital input to the Fix Left and Right RCA output.
6. Press play on the DVD player.
7. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
8. Verify that you hear clean, clear audio coming from the speakers.
9. Pause the DVD and power down the amplifier.
10. In order to test the remaining Digital inputs both RCA and Optical you must move the Digital Input cable to the next Digital input (RCA or Optical), then highlight the input being tested in the Audio I/O Tests Menu and select it by pressing the Right Menu button.
11. Repeat steps 6 - 9 until all the remaining Digital Inputs have been tested.

Digital Input to Record Output Test

This test will verify the path of the #1 Coax Digital input to the Record Fix and Var Left and Right outputs.

1. Connect the digital output source DVD player to the #1 Coax Digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Record Fix outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight S/PDIF Input CX1 Test then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio from the S/PDIF #1 digital input to the Record Fix Left and Right RCA outputs.
6. Press play on the DVD player.
7. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
8. Verify that you hear clean, clear audio coming from the speakers.
9. Pause the DVD and power down the amplifier.
10. Move the cables from the Record Fix Left and Right outputs to the Record Var Left and Right outputs.
11. Power on the amplifier and press play on the DVD player and repeat Steps 6 - 9.

All Remaining Digital Inputs to Record Output Test

This test will verify the path of all of the remaining Digital Coax and Optical Digital inputs to the Record Fix Front Left and Right analog outputs in the test to follow.

1. Connect the digital output source DVD player to the #2 Coax Digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Record Fix outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.

5. Highlight S/PDIF Input CX2 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio from the S/PDIF #2 digital input to the Record Fix Left and Right RCA outputs.
6. Press play on the DVD player.
7. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
8. Verify that you hear clean, clear audio coming from the speakers.
9. Pause the DVD and power down the amplifier.
10. In order to test the remaining Digital inputs (both RCA and Optical) you must move the Digital Input cable to the next Digital input (RCA or Optical), then highlight the input being tested in the Audio I/O Tests Menu and select it by pressing the Right Menu button.
11. Repeat steps 6 - 9 until all the remaining Digital Inputs have been tested.

Digital Input to Digital Outputs Test

This test will verify the path of the S/PDIF #1 Digital input to the Digital S/PDIF outputs (RCA and Optical) of the MC-12/MC-12 Balanced.

1. Connect the digital output source DVD player to the #1 Coax Digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the Coax S/PDIF output on the back of the MC-12/MC-12 Balanced to the digital input of the DAT machine.
3. Connect the Left / Right analog outputs of the DAT to the Analog Left and Right inputs of the amplifier and its outputs to a pair of speakers.
4. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
5. In the Diagnostic Menu, select Audio I/O Tests.
6. Highlight S/PDIF Input Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio from the S/PDIF digital #1 input to both the RCA and Optical S/PDIF digital output connections.
7. Press play on the DVD player.
8. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
9. Verify that you hear clean, clear audio coming from the speakers.
10. Power down the amplifier and MC-12/MC-12 Balanced move the digital cable from the S/PDIF digital output to the Optical S/PDIF digital output.
11. Power on the amplifier and repeat Steps 7 - 9.

All Remaining Digital Inputs to Digital Output Test

This test will verify the path of all remaining Digital Coax and Optical Digital inputs to the S/PDIF RCA digital output.

1. Connect the digital output source DVD player to the #2 Coax Digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the Coax S/PDIF output on the back of the MC-12/MC-12 Balanced to the digital input of the DAT machine.
3. Connect the Left / Right analog outputs of the DAT to the Analog Left and Right inputs of the amplifier and its outputs to a pair of speakers.
4. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
5. In the Diagnostic Menu, select Audio I/O Tests.
6. Highlight S/PDIF Input Test then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio from the S/PDIF digital #2 input to the S/PDIF RCA digital output.
7. Press play on the DVD player.
8. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
9. Verify that you hear clean, clear audio coming from the speakers.
10. In order to test the remaining Digital inputs (both RCA and Optical) to the digital S/PDIF output, you must power down the amplifier and move the Digital Input cable to the next Digital input (RCA or

Optical). Next, highlight the input being tested in the Audio I/O Tests Menu and select it by pressing the Right Menu button.

11. Repeat steps 7 - 9 until all the remaining Digital Inputs have been tested.

AES/EBU Digital Input to all Analog Outputs Test

This test will verify the path of the AES/EBU digital Input to all of the Main analog outputs both RCA and XLR of the MC-12/MC-12 Balanced.

1. Connect the digital output source DVD player to the AES/EBU digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Front outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight AES Input Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio from the AES digital #1 input to both the RCA and XLR.
6. Press play on the DVD player.
7. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
8. Verify that you hear clean, clear audio coming from the speakers.
9. Pause the DVD and power down the amplifier.
10. Move the cables from the Front Left and Right outputs to the Center Left and Right outputs.
11. Power on the amplifier press play on the DVD player and repeat Step 7.
12. Repeat steps 7 - 9 for the remaining paired RCA outputs up to the Left and Right Aux. The Zone 2 and Record outs will be tested later.
13. Remove the RCA output cables from the MC-12/MC-12 Balanced to the amplifier.
14. With a pair of XLR cables connect the Left and Right balanced outputs of the MC-12/MC-12 Balanced to the XLR balanced input of the amplifier.
15. Repeat steps 7 - 9 for the remaining paired XLR balanced outputs up to the Left and Right Aux. As in the RCA test above, the Zone 2 XLR will be tested later.

AES/EBU Digital Input to Zone 2 Output Test

This test will verify the path of the AES/EBU digital input to the Zone 2 Fix and Var RCA and XLR outputs.

1. Connect the digital output source DVD player to the AES/EBU digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Zone 2 Fix outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs, and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight AES Input Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio from the AES digital #1 input to both the RCA and XLR.
6. Press play on the DVD player.
7. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
8. Verify that you hear clean, clear audio coming from the speakers.
9. Pause the DVD and power down the amplifier.
10. Move the cables from the Zone 2 Fix Left and Right outputs to the Zone 2 Var Left and Right outputs.
11. Power on the amplifier, press play on the DVD player, and repeat Steps 7 - 8.
12. Pause the DVD and power down the amplifier.
13. Remove the RCA output cables from the Zone 2 Var Left and Right outputs of the MC-12/MC-12 Balanced to the amplifier.
14. With a pair of XLR cables, connect the Left and Right Zone 2 Fix balanced outputs of the MC-12/MC-12 Balanced to the XLR balanced input of the amplifier.
15. Power on the amplifier, press play on the DVD player, and repeat Step 7 to 9.

AES/EBU Digital Input to Record Output Test

This test will verify path of the AES/EBU digital input to the Record Fix and Var outputs.

1. Connect the digital output source to the AES/EBU digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left and Right Record Fix outputs of the MC-12/MC-12 Balanced to the amplifier Left and Right inputs and the outputs of the amplifier to a pair of speakers.
3. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight AES Input Test then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio from the AES digital #1 input to both the RCA and Fix and Var outputs.
6. Press play on the DVD player.
7. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
8. Verify that you hear clean, clear audio coming from the speakers.
9. Pause the DVD and power down the amplifier.
10. Move the cables from the Record Fix Left and Right outputs to the Record Var Left and Right outputs.
11. Power on the amplifier press play on the DVD player and repeat Steps 7 - 9.

AES/EBU Digital Input to Digital Outputs Test

This test will verify the path of the AES/EBU Digital input to the Digital S/PDIF outputs (RCA and Optical) of the MC-12/MC-12 Balanced.

1. Connect the digital output source to the AES/EBU digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the Coax S/PDIF output on the back of the MC-12/MC-12 Balanced to the digital input of the DAT machine.
3. Connect the Left / Right analog outputs of the DAT to the Analog Left and Right inputs of the amplifier and its outputs to a pair of speakers. If the MC-12/MC-12 Balanced is not in Extended Diagnostics, follow the setup procedure as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight AES Input Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio from the AES digital #1 input to both the RCA and Fix and Var digital outputs.
6. Press play on the DVD player.
7. Slowly increase the volume on the amplifier to a comfortable listening level from the speakers.
8. Verify that you hear clean, clear audio coming from the speakers.
9. Power down the amplifier and MC-12/MC-12 Balanced and move the digital cable from the S/PDIF digital output to the Optical S/PDIF digital output.
10. Power on the amplifier and repeat Steps 6 to 8.

Audio Performance Verification

Performing these tests assures that the audio signal paths in the MC-12/MC-12 Balanced are functional and that the MC-12/MC-12 Balanced meets published specifications. These tests will verify the performance of the A/D and D/A circuitry, gain, frequency response, THD+N, and S/N ratio.

AUDIO INPUTS RCA #1 LEFT AND RIGHT TO ALL LEFT AND RIGHT RCA/XLR OUTPUTS TESTS

This test will verify the specs of the main analog output channels for both RCA and XLRs.

Setup

1. Connect an audio cable between the output of the Low Distortion Oscillator and the MC-12’s Left RCA #1 audio input.

2. Connect an audio cable between the Left Front RCA output of the MC-12/MC-12 Balanced and the input of the Distortion Analyzer.
3. Place the MC-12/MC-12 Balanced into Extended Diagnostics as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight Audio Input 1 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see audio coming in to the Left #1 RCA input to the Front Left RCA output.

Test

1. Apply a 1kHz signal @ 12dBV (+ 4 Vrms) to the input of the MC-12/MC-12 Balanced.
2. Set the scale on the Distortion Analyzer to measure + 12dBV (+4 Vrms) signal level.
3. Turn all the filters off on the Analyzer.
4. Verify that the output level from the MC-12/MC-12 Balanced is +12dBV (+4 Vrms) + 3.71 to 3.45dBV.
5. Adjust the scale on the Distortion Analyzer to measure 0.005% THD-N and turn on the 30kHz low pass or audio bandpass filter.
6. Verify that the THD-N measured is less than 0.003%.
7. Set the scale on the Distortion Analyzer to measure +12dBV (+4 Vrms) signal level.
8. Using the output level from Step 4 above, set for a 0dB reference to check Frequency Response for the MC-12/MC-12 Balanced.
9. Turn the filter on the Analyzer off.
10. Sweep the oscillator frequency from 10Hz to 20kHz.
11. Verify the signal level is within +0.1/-0.25dBV (-0.75dBV @ 40Hz) of the reference level over the entire sweep.
12. Set the scale on the Distortion Analyzer to measure –100dBr signal level with the filter on.
13. Turn off the oscillator to the MC-12/MC-12 Balanced and verify a noise level measurement <-108dBr.
14. Swap cables from the Left #1 RCA input to the Right #1 RCA input and the Left Front RCA output to the Right Front RCA output.
15. Repeat Steps 1 to 13 above.
16. To test the remaining Left and Right RCA / XLR outputs for required specifications, you will need to repeat the above tests using the same RCA #1 Left and Right inputs to the remaining RCA and XLR Left and Right outputs.
17. Repeat steps 1 - 16 again until all the analog outputs are tested.

ALL REMAINING AUDIO RCA INPUTS LEFT AND RIGHT TO FRONT LEFT AND RIGHT RCA OUTPUT TESTS

Setup

1. Connect an audio cable between the output of the Low Distortion Oscillator and the MC-12's Left RCA #2 audio input.
2. Connect an audio cable between the Center RCA output of the MC-12/MC-12 Balanced and the input of the Distortion Analyzer.
3. Place the MC-12/MC-12 Balanced into Extended Diagnostics as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight Audio Input 2 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see audio coming in to the Left and Right #2 RCA input to the Front Left and Right RCA output and all the remaining RCA and XLR paired Left and Right audio output connections.

Test

1. Apply a 1kHz signal @+12dBV (+4 Vrms) to the input of the MC-12/MC-12 Balanced.
2. Set the scale on the Distortion Analyzer to measure +12dBV (+4 Vrms) signal level.
3. Turn all the filters off on the Analyzer.
4. Verify that the output level from the MC-12/MC-12 Balanced is +12dBV (+4 Vrms) + 3.71 to 3.45dBV.
5. Adjust the scale on the Distortion Analyzer to measure 0.005% THD-N and turn on the 30kHz low pass or audio bandpass filter.

6. Verify that the THD-N measured is less than 0.003%.
7. Set the scale on the Distortion Analyzer to measure +12 dBV (+4 Vrms) signal level.
8. Using the output level from Step 4 above, set for a 0dB reference to check Frequency Response for the MC-12/MC-12 Balanced.
9. Turn the filter on the Analyzer off.
10. Sweep the oscillator frequency from 10Hz to 20kHz.
11. Verify the signal level is within +0.1/-0.25dBV (–0.75dBV @ 40Hz) of the of reference level over the entire sweep.
12. Set the scale on the Distortion Analyzer to measure –100dBr signal level with the filter on.
13. Turn off the oscillator to the MC-12/MC-12 Balanced and verify a noise level measurement <-108dBr.
14. Swap cables from the Left #2 RCA input to the Right #2 RCA input and the Left Front RCA output to the Right Front RCA output.
15. Repeat Steps 1 - 13 above.
16. To test all the remaining Left and Right RCA inputs for required specifications you will need to repeat Step 5 in the Setup section and engage the next Audio Input Test in the diagnostic menu.
17. Repeat steps 1 - 14.

AUDIO INPUTS RCA #1 LEFT AND RIGHT TO ZONE 2 LEFT AND RIGHT RCA FIX /VAR OUTPUTS AND ZONE 2 XLR OUTPUTS TESTS

Setup

1. Connect an audio cable between the output of the Low Distortion Oscillator and the MC-12's Left RCA #1 audio input.
2. Connect an audio cable between the Zone 2 Left Fix RCA output of the MC-12/MC-12 Balanced and the input of the Distortion Analyzer.
3. Place the MC-12/MC-12 Balanced into Extended Diagnostics as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight Audio Input 1 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see audio coming in to the Left #1 RCA input to the Zone 2 Left Fix RCA output.

Tests

1. Apply a 1kHz signal @+12dBV (+4 Vrms) to the input of the MC-12/MC-12 Balanced.
2. Set the scale on the Distortion Analyzer to measure +12dBV (+4 Vrms) signal level.
3. Turn all the filters off on the Analyzer.
4. Verify that the output level from the MC-12/MC-12 Balanced is +12dBV (+4 Vrms) + 3.71 to 3.45dBV.
5. Adjust the scale on the Distortion Analyzer to measure 0.005% THD-N and turn on the 30kHz low pass or audio bandpass filter.
6. Verify that the THD-N measured is less than 0.003%.
7. Set the scale on the Distortion Analyzer to measure +12 dBV (+4 Vrms) signal level.
8. Using the output level from Step 4 above, set for a 0dB reference to check Frequency Response for the MC-12/MC-12 Balanced.
9. Turn the filter on the Analyzer off.
10. Sweep the oscillator frequency from 10Hz to 20kHz.
11. Verify the signal level is within +0.1/-0.25dBV (–0.75dBV @ 40Hz) of the reference level over the entire sweep.
12. Set the scale on the Distortion Analyzer to measure –100dBr signal level with the filter on.
13. Turn off the oscillator to the MC-12/MC-12 Balanced and verify a noise level measurement <-108dBr.
14. Swap cables from the Left #1 input to the Right #1 input and the Left Fix RCA output to the Right Fix RCA output.
15. Repeat Steps 1 - 11 above.
16. Test the Zone 2 RCA Var outputs and the XLR Zone 2 outputs using the above test.

AUDIO INPUTS RCA #1 LEFT AND RIGHT TO RECORD LEFT AND RIGHT RCA FIX /VAR OUTPUTS TESTS

Setup

1. Connect an audio cable between the output of the Low Distortion Oscillator and the MC-12's Left RCA #1 audio input.
2. Connect an audio cable between the Record Left Fix RCA output of the MC-12/MC-12 Balanced and the input of the Distortion Analyzer.
3. Place the MC-12/MC-12 Balanced into Extended Diagnostics as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight Audio Input 1 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see audio coming in to the Left #1 RCA input to the Record Left Fix RCA output.

Tests

1. Apply a 1kHz signal @+12dBV (+4 Vrms) to the input of the MC-12/MC-12 Balanced.
2. Set the scale on the Distortion Analyzer to measure +12dBV (+4 Vrms) signal level.
3. Turn all the filters off on the Analyzer.
4. Verify that the output level from the MC-12/MC-12 Balanced is +12dBV (+4 Vrms) +3.71 to 3.45dBV.
5. Adjust the scale on the Distortion Analyzer to measure 0.005% THD-N and turn on the 30kHz low pass or audio bandpass filter.
6. Verify that the THD-N measured is less than 0.003%.
7. Set the scale on the Distortion Analyzer to measure +12 dBV (+4 Vrms) signal level.
8. Using the output level from Step 4 above set for a 0dB reference to check Frequency Response for the MC-12/MC-12 Balanced.
9. Turn the filter on the Analyzer off.
10. Sweep the oscillator frequency from 10Hz to 20kHz.
11. Verify the signal level is within +0.1/-0.25dBV (–0.75dBV @ 40Hz) of the reference level over the entire sweep.
12. Set the scale on the Distortion Analyzer to measure –100dBr signal level with the filter on.
13. Turn off the oscillator to the MC-12/MC-12 Balanced and verify a noise level measurement <-108dBr.
14. Swap cables from the Left #1 input to the Right #1 input and the Left Record Fix output to the Right Record Fix output.
15. Repeat Steps 1 - 13 above.
16. Repeat the test above for the Left and Right Record Var outputs.

ALL DIGITAL AUDIO INPUTS COAX, OPTICAL, AES/EBU TO THE LEFT AND RIGHT FRONT RCA OUTPUTS TESTS

Having tested all Analog to Analog specifications in the above tests, it is now only necessary to prove that all the Digital inputs pass specifications. This test will verify the specifications of all Digital Inputs to the Front Left and Right RCA outputs.

Setup

1. Connect the digital output source to the #1 Coax digital input on the rear panel of the MC-12/MC-12 Balanced.
2. Connect the RCA Left Front output of the MC-12/MC-12 Balanced to the amplifier Left inputs and the output of the amplifier to a pair of speakers.
3. Place the MC-12/MC-12 Balanced into Extended Diagnostics as described at the beginning of this chapter.
4. In the Diagnostic Menu, select Audio I/O Tests.
5. Highlight S/PDIF Input CX1 Test, then press the Right menu button to engage the test. The MC-12/MC-12 Balanced is now set to see digital audio from the S/PDIF #1 digital input to the Front Left and Right RCA output and all the remaining RCA and XLR paired Left and Right audio output connections.

Tests

1. Apply a 1kHz signal @ +0.00dBFS to the input of the MC-12/MC-12 Balanced.
2. Set the scale on the Distortion Analyzer to measure +12dBV (+4 Vrms) signal level.
3. Turn all the filters off on the Analyzer.
4. Verify that the output level from the MC-12/MC-12 Balanced is +12dBV (+4 Vrms) +4.025 to 3.590dBV.
5. Adjust the scale on the Distortion Analyzer to measure 0.005% THD-N and turn on the 30kHz low pass or audio bandpass filter.
6. Verify that the THD-N measured is less than 0.003%.
7. Set the scale on the Distortion Analyzer to measure +12 dBV (+4 Vrms) signal level.
8. Using the output level from Step 4 above set for a 0dB reference to check Frequency Response for the MC-12/MC-12 Balanced.
9. Turn the filter on the Analyzer off.
10. Sweep the oscillator frequency from 10hz to 20kHz.
11. Verify the signal level is within +0.1/-0.25dBV (–0.75dBV @ 40Hz) of the reference level over the entire sweep.
12. Set the scale on the Distortion Analyzer to measure –100dBr signal level with the filter on.
13. Turn off the oscillator to the MC-12/MC-12 Balanced and verify a noise level measurement <-108dBr.
14. Swap cables from the Coax #1 Digital input to the Coax #2 Digital input.
15. To test all the remaining Left and Right RCA inputs for required specifications you will need to repeat Step 5 in the Setup section and engage the next Audio Input Test in the diagnostic menu.
16. Repeat steps 1 - 13.

Video Input / Output Tests

These tests will verify that all 17 video inputs and 9 outputs pass video. There are 3 different types of video to be tested in the MC-12/MC-12 Balanced: Composite - 5 Input and 4 Outputs; S-Video - 8 Inputs and 4 Outputs; Component - 4 Inputs and 1 Output. The following tests, will verify that the MC-12/MC-12 Balanced is passing clear, clean video to it source. It is not necessary to enter the Extended Diagnostics as we did in the Audio tests to perform the Video tests.

COMPOSITE INPUTS TO COMPOSITE (MAIN AND RECORD) OUTPUTS TESTS

This test will set up a simple pass through of Video information in order to verify the Composite video switching properties of the MC-12/MC-12 Balanced.

Setup

1. Connect the Composite video output from the DVD to the MC-12's #1 Composite video input.
2. Connect the Composite video #1 Main output of the MC-12/MC-12 Balanced to the Monitor's Composite video Input.
3. Turn on the DVD, Monitor, and MC-12/MC-12 Balanced.
4. The Monitor should have a blue screen display.
5. On the MC-12/MC-12 Balanced remote, press the DVD-1 button to select this as the Input for testing the video paths.
6. Press the Menu button on the remote. The Main Menu should appear on the screen.
7. With the Down Menu button on the remote, scroll down to SETUP, then select by pressing the Right Menu button.
8. The SETUP Menu will appear and the INPUTS at the top will be highlighted. At this point press the Right Menu button again.
9. The INPUT SETUP Menu will appear. At the top will be DVD1. To keep things simple, use this DVD1 Input to test all the video inputs and outputs of the MC-12/MC-12 Balanced.
10. Press the Right Menu button. The MC-12/MC-12 Balanced will now be set to the DVD1 INPUT SETUP Menu.
11. Using Down button scroll down to the VIDEO IN S-VIDEO-1 and press the Right Menu button.
12. Select any of the 5 Composite or 8 S-Video Inputs of the MC-12/MC-12 Balanced from the DVD1 Video In Menu.

13. Scroll to the COMPOSITE-1 Video input and press the Right Menu button. This will assign the Composite Video input 1 Jack to all composite Video output jacks, both in Main and Record of the MC-12/MC-12 Balanced.
14. Press the OSD button on the remote. This will turn off the on-screen video information from the MC-12/MC-12 Balanced and allow you to view the video for the DVD. The video path is now set for testing.

Test

1. Load a disc into the DVD player and press play.
2. Verify a clean, undistorted picture appears on the screen.
3. Pause the DVD.
4. Test the remaining Composite outputs by switching the Composite output cable to Main2 and Record 1, 2 and repeating steps 1 - 3 above.
5. Pause the player.
6. To test the remaining Composite video inputs of the MC-12/MC-12 Balanced, leave the Composite Video output on Record 2 output.
7. Switch from the Composite-1 input to the Composite-2 input.
8. Select the Composite-2 to 5 in the DVD1 VIDEO IN Menu as stated in the Setup section above, then repeat steps 1 to 3 above.

S-VIDEO INPUTS TO S-VIDEO (MAIN AND RECORD) OUTPUTS TESTS

This test will set up a simple pass through of Video information in order to verify the S-Video switching properties of the MC-12/MC-12 Balanced.

Setup

1. Connect the S-Video output from the DVD to the MC-12's #1 S-Video input.
2. Connect the S-Video #1 Main output of the MC-12/MC-12 Balanced to the Monitors S-Video Input.
3. Turn on the DVD, Monitor, and MC-12/MC-12 Balanced.
4. The Monitor should have a blue screen display.
5. On the MC-12/MC-12 Balanced remote, press the DVD-1 button to select this as our Input for testing the video paths.
6. Press the Menu button on the remote. The Main Menu should appear on the screen.
7. With the Down Menu button on the remote, scroll down to SETUP, then select by pressing the Right Menu button.
8. The SETUP Menu will appear and the INPUTS at the top will be highlighted. At this point press the Right Menu button again.
9. The INPUT SETUP Menu will appear. At the top will be DVD1. To keep things simple, use this DVD1 Input to test all the video input and outputs of the MC-12/MC-12 Balanced.
10. Press the Right Menu button. The MC-12/MC-12 Balanced will now be set to the DVD1 INPUT SETUP Menu.
11. Using Down button scroll down to the VIDEO IN S-VIDEO-1 and press the Right Menu button.
12. In the DVD1 VIDEO IN Menu, select any of the 8 S-Video Inputs of the MC-12/MC-12 Balanced to be tested by scrolling down to it and selecting the video path to be tested by pressing the Right Menu button.
13. At this time the MC-12/MC-12 Balanced is already set to S-Video-1 input to all the S-video outputs (Main 1, 2 and Record 1, 2) of the MC-12/MC-12 Balanced.
14. Press the OSD button on the remote. This will turn off the on-screen video information from the MC-12/MC-12 Balanced and allow you to view the video for the DVD The video path is now set for testing.

Test

1. Load a disc into the DVD player and press play.
2. Verify a clean, undistorted picture appears on the screen.
3. Pause the player.
4. Test the remaining S-Video outputs by switching the S-Video output cable to Main2 and Record 1, 2 and repeating steps 1 - 3 above.
5. Pause the DVD player.

6. To test the remaining S-Video inputs of the MC-12/MC-12 Balanced, leave the S-Video output on Record 2 output.
7. Switch from the S-Video-1 input to the S-Video-2 input.
8. You must select the S-Video 2 - 8 in the DVD1 VIDEO IN Menu as stated in the Setup section above, then repeat steps 1 - 3 above.

COMPONENT INPUTS TO COMPONENT OUTPUT TESTS

This test will set up a simple pass through of Video information in order to verify the Component video switching properties of the MC-12/MC-12 Balanced.

Setup

1. Connect the 3-wire Component Video output from the DVD to the MC-12's Component Video #1 input.
2. Connect the 3-wire Component BNC video outputs of the MC-12/MC-12 Balanced to the Monitor's BNC Component Video Inputs.
3. Turn on the DVD, Monitor, and MC-12/MC-12 Balanced.
4. The Monitor should have a blue screen display.
5. On the MC-12/MC-12 Balanced remote, press the DVD-1 button to select this as the Input for testing the video paths.
6. Press the Menu button on the remote. The Main Menu should appear on the screen.
7. With the Down Menu button on the remote, scroll down to SETUP, then select by pressing the Right Menu button.
8. The SETUP Menu will appear and the INPUTS at the top will be highlighted. At this point press the Right Menu button again.
9. The INPUT SETUP Menu will appear. At the top will be DVD1. To keep things simple, use this DVD1 Input to test all the video input and outputs of the MC-12/MC-12 Balanced.
10. Press the Right Menu button. The MC-12/MC-12 Balanced will now be set to the DVD1 INPUT SETUP Menu.
11. Using Down button scroll down to the COMPONENT IN and press the Right Menu button.
12. In the DVD1 COMPONENT Menu, select any of the 4 COMPONENT Video Inputs of the MC-12/MC-12 Balanced to be tested.
13. At this time the MC-12/MC-12 Balanced is already set to COMPONENT 1 Video input to the COMPONENT Video output of the MC-12/MC-12 Balanced.
14. Press the OSD button on the remote. This will turn off the on-screen video information from the MC-12/MC-12 Balanced and allow you to view the video for the DVD. The video path is now set for testing.

Test

1. Load a disc into the DVD and press play.
2. Verify a clean, undistorted picture appears on the screen.
3. Pause the tape.
4. Test the remaining COMPONENT Video inputs of the MC-12/MC-12 Balanced, switch the COMPONENT Video input cable to 2, 3, and 4 and repeat steps 1 - 3 above.
5. Pause the player after testing Component Video #3.
6. Remove the 3-wire RCA Component Video cable that connects the video output from the DVD player to the back of the MC-12/MC-12 Balanced.
7. Using the 3-wire BNC Video cable, connect the Component Video output of the DVD player to the MC-12/MC-12 Balanced Component #4 video input.
8. Press play on the DVD player.
9. Verify a clean, undistorted picture appears on the screen.

LEXICON AUDIO PRECISION ATE SUMMARY

This chart represents a summary of Audio Precision test settings and parameters used by Lexicon in production testing of all MC-12/MC-12 Balanced products. This is provided as a reference and supplement to bench test settings found in the proof of performance section in this manual.

A-D Tests	Generator						Analyzer								MC-12 Setup		
Test Name	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	Clock Source	Sample Rate	Audio Source
ANLG_REC_IN1_TO_DIG_REC_COAX_OUT_96K																	
ANLG_REC_IN1_TO_DIG_REC_COAX_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN1_TO_DIG_REC_COAX_OUT_96K_FREQ	2.00Vrms	2.00Vrms	10-40k	20	Unbal	Float	dBr	Level	+0.00/-0.04	+0.10	-0.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN1_TO_DIG_REC_COAX_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN1_TO_DIG_REC_COAX_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN1_TO_DIG_REC_COAX_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_REC_IN2_TO_DIG_REC_COAX_OUT_96K																	
ANLG_REC_IN2_TO_DIG_REC_COAX_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN2_TO_DIG_REC_COAX_OUT_96K_FREQ	2.00Vrms	2.00Vrms	10-40k	20	Unbal	Float	dBr	Level	+0.00/-0.04	+0.10	-0.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN2_TO_DIG_REC_COAX_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN2_TO_DIG_REC_COAX_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN2_TO_DIG_REC_COAX_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_REC_IN3_TO_DIG_REC_COAX_OUT_96K																	
ANLG_REC_IN3_TO_DIG_REC_COAX_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN3_TO_DIG_REC_COAX_OUT_96K_FREQ	2.00Vrms	2.00Vrms	10-40k	20	Unbal	Float	dBr	Level	+0.00/-0.04	+0.10	-0.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN3_TO_DIG_REC_COAX_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN3_TO_DIG_REC_COAX_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN3_TO_DIG_REC_COAX_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_REC_IN4_TO_DIG_REC_COAX_OUT_96K																	
ANLG_REC_IN4_TO_DIG_REC_COAX_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN4_TO_DIG_REC_COAX_OUT_96K_FREQ	2.00Vrms	2.00Vrms	10-40k	20	Unbal	Float	dBr	Level	+0.00/-0.04	+0.10	-0.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN4_TO_DIG_REC_COAX_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN4_TO_DIG_REC_COAX_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN4_TO_DIG_REC_COAX_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_REC_IN5_TO_DIG_REC_COAX_OUT_96K																	
ANLG_REC_IN5_TO_DIG_REC_COAX_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN5_TO_DIG_REC_COAX_OUT_96K_FREQ	2.00Vrms	2.00Vrms	10-40k	20	Unbal	Float	dBr	Level	+0.00/-0.04	+0.10	-0.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN5_TO_DIG_REC_COAX_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN5_TO_DIG_REC_COAX_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN5_TO_DIG_REC_COAX_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_REC_IN6_TO_DIG_REC_COAX_OUT_96K																	
ANLG_REC_IN6_TO_DIG_REC_COAX_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN6_TO_DIG_REC_COAX_OUT_96K_FREQ	2.00Vrms	2.00Vrms	10-40k	20	Unbal	Float	dBr	Level	+0.00/-0.04	+0.10	-0.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN6_TO_DIG_REC_COAX_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN6_TO_DIG_REC_COAX_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN6_TO_DIG_REC_COAX_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_REC_IN7_TO_DIG_REC_COAX_OUT_96K																	
ANLG_REC_IN7_TO_DIG_REC_COAX_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN7_TO_DIG_REC_COAX_OUT_96K_FREQ	2.00Vrms	2.00Vrms	10-40k	20	Unbal	Float	dBr	Level	+0.00/-0.04	+0.10	-0.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN7_TO_DIG_REC_COAX_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN7_TO_DIG_REC_COAX_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN7_TO_DIG_REC_COAX_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_REC_IN8_TO_DIG_REC_COAX_OUT_96K																	
ANLG_REC_IN8_TO_DIG_REC_COAX_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN8_TO_DIG_REC_COAX_OUT_96K_FREQ	2.00Vrms	2.00Vrms	10-40k	20	Unbal	Float	dBr	Level	+0.00/-0.04	+0.10	-0.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN8_TO_DIG_REC_COAX_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN8_TO_DIG_REC_COAX_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_REC_IN8_TO_DIG_REC_COAX_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_REC_IN1_TO_DIG_REC_OPT_OUT_88K																	
ANLG_REC_IN1_TO_DIG_REC_OPT_OUT_88K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	88000	Analog
ANLG_REC_IN1_TO_DIG_REC_OPT_OUT_88K_THD	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	THD+N	<-93.00	-88.00	-120.00	None	n/a	<10 - Fs/2	Internal	88000	Analog
ANLG_REC_IN1_TO_DIG_REC_OPT_OUT_88K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	88000	Analog
ANLG_REC_IN1_TO_DIG_REC_OPT_OUT_48K																	
ANLG_REC_IN1_TO_DIG_REC_OPT_OUT_48K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	48000	Analog
ANLG_REC_IN1_TO_DIG_REC_OPT_OUT_48K_THD	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	THD+N	<-95.00	-88.00	-120.00	None	n/a	<10 - Fs/2	Internal	48000	Analog
ANLG_REC_IN1_TO_DIG_REC_OPT_OUT_48K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	48000	Analog
ANLG_REC_IN1_TO_DIG_REC_OPT_OUT_44K																	
ANLG_REC_IN1_TO_DIG_REC_OPT_OUT_44K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	44100	Analog
ANLG_REC_IN1_TO_DIG_REC_OPT_OUT_44K_THD	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	THD+N	<-95.00	-88.00	-120.00	None	n/a	<10 - Fs/2	Internal	44100	Analog
ANLG_REC_IN1_TO_DIG_REC_OPT_OUT_44K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	44100	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_96K																	
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_ZONE_IN2_TO_DIG_REC_OPT_OUT_96K																	
ANLG_ZONE_IN2_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN2_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN2_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN2_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog

A-D Tests	Analog Generator						Digital Analyzer										
Test Name	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	Clock Source	Sample Rate	Audio Source
ANLG_ZONE_IN3_TO_DIG_REC_OPT_OUT_96K																	
ANLG_ZONE_IN3_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN3_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN3_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN3_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_ZONE_IN4_TO_DIG_REC_OPT_OUT_96K																	
ANLG_ZONE_IN4_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN4_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN4_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN4_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_ZONE_IN5_TO_DIG_REC_OPT_OUT_96K																	
ANLG_ZONE_IN5_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN5_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN5_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN5_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_ZONE_IN6_TO_DIG_REC_OPT_OUT_96K																	
ANLG_ZONE_IN6_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN6_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN6_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN6_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_ZONE_IN7_TO_DIG_REC_OPT_OUT_96K																	
ANLG_ZONE_IN7_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN7_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN7_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN7_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_ZONE_IN8_TO_DIG_REC_OPT_OUT_96K																	
ANLG_ZONE_IN8_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN8_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-93.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN8_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_ZONE_IN8_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_88K																	
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_88K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	88000	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_88K_THD	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	THD+N	<-93.00	-88.00	-120.00	None	n/a	<10 - Fs/2	Internal	88000	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_88K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	88000	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_48K																	
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_48K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	48000	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_48K_THD	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	THD+N	<-95.00	-88.00	-120.00	None	n/a	<10 - Fs/2	Internal	48000	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_48K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	48000	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_44K																	
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_44K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	44100	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_44K_THD	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	THD+N	<-95.00	-88.00	-120.00	None	n/a	<10 - Fs/2	Internal	44100	Analog
ANLG_ZONE_IN1_TO_DIG_REC_OPT_OUT_44K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	44100	Analog
ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_96K																	
ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-92.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_MAIN_IN2_TO_DIG_REC_OPT_OUT_96K																	
ANLG_MAIN_IN2_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN2_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-92.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN2_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN2_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_MAIN_IN3_TO_DIG_REC_OPT_OUT_96K																	
ANLG_MAIN_IN3_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN3_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-92.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN3_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN3_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_MAIN_IN4_TO_DIG_REC_OPT_OUT_96K																	
ANLG_MAIN_IN4_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN4_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-92.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN4_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN4_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_MAIN_IN5_TO_DIG_REC_OPT_OUT_96K																	
ANLG_MAIN_IN5_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN5_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-92.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN5_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN5_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
ANLG_MAIN_IN6_TO_DIG_REC_OPT_OUT_96K																	
ANLG_MAIN_IN6_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN6_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-92.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN6_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
ANLG_MAIN_IN6_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog

	A-D Tests	Analog Generator						Digital Analyzer										
	Test Name	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	Clock Source	Sample Rate	Audio Source
	ANLG_MAIN_IN7_TO_DIG_REC_OPT_OUT_96K																	
	ANLG_MAIN_IN7_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
	ANLG_MAIN_IN7_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-92.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
	ANLG_MAIN_IN7_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
	ANLG_MAIN_IN7_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
	ANLG_MAIN_IN8_TO_DIG_REC_OPT_OUT_96K																	
	ANLG_MAIN_IN8_TO_DIG_REC_OPT_OUT_96K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	96000	Analog
	ANLG_MAIN_IN8_TO_DIG_REC_OPT_OUT_96K_THD	4.00Vrms	4.00Vrms	20-1k/5k-40k	20	Unbal	Float	dBFS	THD+N	<-92.00/-78.00	-88.00/-75.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
	ANLG_MAIN_IN8_TO_DIG_REC_OPT_OUT_96K_XTALK	4.00Vrms	4.00Vrms	15k	20	Unbal	Float	dB	Level	-88.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
	ANLG_MAIN_IN8_TO_DIG_REC_OPT_OUT_96K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	96000	Analog
	ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_88K																	
	ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_88K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	88000	Analog
	ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_88K_THD	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	THD+N	<-93.00	-88.00	-120.00	None	n/a	<10 - Fs/2	Internal	88000	Analog
	ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_88K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	88000	Analog
	ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_48K																	
	ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_48K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	48000	Analog
	ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_48K_THD	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	THD+N	<-95.00	-88.00	-120.00	None	n/a	<10 - Fs/2	Internal	48000	Analog
	ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_48K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	48000	Analog
	ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_44K																	
	ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_44K_GAIN	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	Level	-0.66	+0.00	-1.10	None	n/a	<10 - Fs/2	Internal	44100	Analog
	ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_44K_THD	4.00Vrms	4.00Vrms	997	20	Unbal	Float	dBFS	THD+N	<-95.00	-88.00	-120.00	None	n/a	<10 - Fs/2	Internal	44100	Analog
	ANLG_MAIN_IN1_TO_DIG_REC_OPT_OUT_44K_DYNRNG	4.00mVrms	4.00mVrms	997	20	Unbal	Float	dBFS	THD+N	-106.00	-104.00	-130.00	Narrow	n/a	<10Hz->20kHz LP	Internal	44100	Analog
	ANLG_MAIN_MIC_IN1&2_TO_DIG_REC_OPT_OUT_96K																	
	ANLG_MAIN_MIC_IN1&2_TO_DIG_REC_OPT_OUT_96K_GAIN	50mVrms	50mVrms	997	40	Bal	Float	dBFS	Level	-5.76	-5.21	-6.31	None	n/a	<10 - Fs/2	Internal	96000	Analog
	ANLG_MAIN_MIC_IN1&2_TO_DIG_REC_OPT_OUT_96K_FREQ	50mVrms	50mVrms	20-20k	40	Bal	Float	dBr	Level	<+0.00/-0.25	+0.10	-0.50	None	n/a	<10 - Fs/2	Internal	96000	Analog
	ANLG_MAIN_MIC_IN1&2_TO_DIG_REC_OPT_OUT_96K_THD	50mVrms	50mVrms	997	40	Bal	Float	dBFS	THD+N	<-74.00	-70.00	-120.00	None	n/a	22Hz->20kHz LP	Internal	96000	Analog
	ANLG_MAIN_MIC_IN3&4_TO_DIG_REC_OPT_OUT_96K																	
	ANLG_MAIN_MIC_IN3&4_TO_DIG_REC_OPT_OUT_96K_GAIN	50mVrms	50mVrms	997	40	Bal	Float	dBFS	Level	-5.76	-5.21	-6.31	None	n/a	<10 - Fs/2	Internal	96000	Analog
	ANLG_MAIN_MIC_IN3&4_TO_DIG_REC_OPT_OUT_96K_FREQ	50mVrms	50mVrms	20-20k	40	Bal	Float	dBr	Level	<+0.00/-0.25	+0.10	-0.50	None	n/a	<10 - Fs/2	Internal	96000	Analog
	ANLG_MAIN_MIC_IN3&4_TO_DIG_REC_OPT_OUT_96K_THD	50mVrms	50mVrms	997	40	Bal	Float	dBFS	THD+N	<-74.00	-70.00	-120.00	None	n/a	22Hz->20kHz LP	Internal	96000	Analog
	ANLG_MAIN_MIC_IN3&4_TO_DIG_REC_OPT_OUT_96K_ADMUX																	
	ANLG_MAIN_MIC_IN3&4_TO_DIG_REC_OPT_OUT_96K_ADMUX	50mVrms	50mVrms	997	40	Bal	Float	dBFS	Level	<-87.00	-80.00	-120.00	None	n/a	<10 - Fs/2	Internal	96000	Analog
	Note: ADMUX = MIC Inputs 3&4 are disabled while being driven at 4.00 mVrms																	

	D-A Tests	Digital Generator						Analog Analyzer										
	Test Name	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	Clock Source	Sample Rate	Audio Source
	DIG_REC_COAX1_IN_96K_TO_ANLG_REC_FIX_OUT																	
141	DIG_REC_COAX1_IN_96K_TO_ANLG_REC_FIX_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+3.83	+4.025	+3.590	40kHz LP	100k	<10 - >500k	External	96000	Digital
142	DIG_REC_COAX1_IN_96K_TO_ANLG_REC_FIX_OUT_FREQ	-1.00dBFS	-1.00dBFS	10-20k/40k	n/a	n/a	n/a	dBr	Level	<-0.07/-0.39	+0.10	-0.25/-0.75	None	100k	<10 - >500k	External	96000	Digital
143	DIG_REC_COAX1_IN_96K_TO_ANLG_REC_FIX_OUT_THD	-1.00dBFS	-1.00dBFS	20-1k/5k-8k/10k-40k	n/a	n/a	n/a	%	THD+N	<.002/.009/.025	.005/.010/.030	.0002	40kHz LP	100k	<10 - >500k	External	96000	Digital
144	DIG_REC_COAX1_IN_96K_TO_ANLG_REC_FIX_OUT_XTALK	-1.00dBFS	-1.00dBFS	15k	n/a	n/a	n/a	dB	Level	>-90.00	-80.00	-150.00	None	100k	<10 - 22k	External	96000	Digital
145	DIG_REC_COAX1_IN_96K_TO_ANLG_REC_FIX_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-105.00	-140.00	None	100k	<10 - 22k	External	96000	Digital
	DIG_REC_COAX1_IN_88K_TO_ANLG_REC_FIX_OUT																	
146	DIG_REC_COAX1_IN_88K_TO_ANLG_REC_FIX_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+3.83	+4.025	+3.590	40kHz LP	100k	<10 - >500k	External	88000	Digital
147	DIG_REC_COAX1_IN_88K_TO_ANLG_REC_FIX_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	40kHz LP	100k	<10 - >500k	External	88000	Digital
148	DIG_REC_COAX1_IN_88K_TO_ANLG_REC_FIX_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-105.00	-140.00	None	100k	<10 - 22k	External	88000	Digital
	DIG_REC_COAX1_IN_48K_TO_ANLG_REC_FIX_OUT																	
149	DIG_REC_COAX1_IN_48K_TO_ANLG_REC_FIX_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+3.83	+4.025	+3.590	40kHz LP	100k	<10 - >500k	External	48000	Digital
150	DIG_REC_COAX1_IN_48K_TO_ANLG_REC_FIX_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	40kHz LP	100k	<10 - >500k	External	48000	Digital
151	DIG_REC_COAX1_IN_48K_TO_ANLG_REC_FIX_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-105.00	-140.00	None	100k	<10 - 22k	External	48000	Digital
	DIG_REC_COAX1_IN_44K_TO_ANLG_REC_FIX_OUT																	
152	DIG_REC_COAX1_IN_44K_TO_ANLG_REC_FIX_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+3.83	+4.025	+3.590	40kHz LP	100k	<10 - >500k	External	44100	Digital
153	DIG_REC_COAX1_IN_44K_TO_ANLG_REC_FIX_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital
154	DIG_REC_COAX1_IN_44K_TO_ANLG_REC_FIX_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-105.00	-140.00	None	100k	<10 - 22k	External	44100	Digital
	DIG_REC_COAX1_IN_44K_TO_ANLG_REC_VAR_OUT																	
155	DIG_REC_COAX1_IN_44K_TO_ANLG_REC_VAR_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+3.83	+4.025	+3.590	40kHz LP	100k	<10 - >500k	External	44100	Digital
156	DIG_REC_COAX1_IN_44K_TO_ANLG_REC_VAR_OUT_FREQ	-1.00dBFS	-1.00dBFS	10-20k/40k	n/a	n/a	n/a	dBr	Level	<-0.07/-0.39	+0.10	-0.25/-0.75	None	100k	<10 - >500k	External	44100	Digital
157	DIG_REC_COAX1_IN_44K_TO_ANLG_REC_VAR_OUT_THD	-1.00dBFS	-1.00dBFS	20-1k/5k-8k/10k-40k	n/a	n/a	n/a	%	THD+N	<.002/.009/.025	.005/.010/.030	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital
158	DIG_REC_COAX1_IN_44K_TO_ANLG_REC_VAR_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-105.00	-140.00	None	100k	<10 - 22k	External	44100	Digital
	DIG_REC_COAX1_IN_96K_TO_ANLG_REC_VAR_OUT_AADIRMUX																	
159	DIG_REC_COAX1_IN_96K_TO_ANLG_REC_VAR_OUT_AADIRMUX	OFF *	OFF *	997	20	Unbal	Float	Vrms	Level	>-78.00	-72.00	-140.00	40kHz LP	100k		External	96000	Digital
	** AADIRMUX = Analog Record Inputs are driven at 4.0Vrms with only the Digital Record Input selected.*																	

	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_FIX_OUT																	
160	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_FIX_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+3.83	+4.025	+3.590	40kHz LP	100k	<10 - >500k	External	96000	Digital
161	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_FIX_OUT_FREQ	-1.00dBFS	-1.00dBFS	10-20k/40k	n/a	n/a	n/a	dBr	Level	<-0.07/-0.39	+0.10	-0.25/-0.75	None	100k	<10 - >500k	External	96000	Digital
162	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_FIX_OUT_THD	-1.00dBFS	-1.00dBFS	20-1k/5k-8k/10k-40k	n/a	n/a	n/a	%	THD+N	<.002/.009/.025	.005/.010/.030	.0002	40kHz LP	100k	<10 - >500k	External	96000	Digital
163	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_FIX_OUT_XTALK	-1.00dBFS	-1.00dBFS	15k	n/a	n/a	n/a	dB	Level	>-90.00	-80.00	-150.00	None	100k	<10 - 22k	External	96000	Digital
164	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_FIX_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-105.00	-140.00	None	100k	<10 - 22k	External	96000	Digital
	DIG_ZONE_COAX1_IN_88K_TO_ANLG_ZONE_FIX_OUT																	
165	DIG_ZONE_COAX1_IN_88K_TO_ANLG_ZONE_FIX_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+3.83	+4.025	+3.590	40kHz LP	100k	<10 - >500k	External	88000	Digital
166	DIG_ZONE_COAX1_IN_88K_TO_ANLG_ZONE_FIX_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	40kHz LP	100k	<10 - >500k	External	88000	Digital
167	DIG_ZONE_COAX1_IN_88K_TO_ANLG_ZONE_FIX_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-105.00	-140.00	None	100k	<10 - 22k	External	88000	Digital
	DIG_ZONE_COAX1_IN_48K_TO_ANLG_ZONE_FIX_OUT																	
168	DIG_ZONE_COAX1_IN_48K_TO_ANLG_ZONE_FIX_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+3.83	+4.025	+3.590	40kHz LP	100k	<10 - >500k	External	48000	Digital
169	DIG_ZONE_COAX1_IN_48K_TO_ANLG_ZONE_FIX_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	40kHz LP	100k	<10 - >500k	External	48000	Digital
170	DIG_ZONE_COAX1_IN_48K_TO_ANLG_ZONE_FIX_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-105.00	-140.00	None	100k	<10 - 22k	External	48000	Digital
	DIG_ZONE_COAX1_IN_44K_TO_ANLG_ZONE_FIX_OUT																	
171	DIG_ZONE_COAX1_IN_44K_TO_ANLG_ZONE_FIX_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+3.83	+4.025	+3.590	40kHz LP	100k	<10 - >500k	External	44100	Digital
172	DIG_ZONE_COAX1_IN_44K_TO_ANLG_ZONE_FIX_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital
173	DIG_ZONE_COAX1_IN_44K_TO_ANLG_ZONE_FIX_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-105.00	-140.00	None	100k	<10 - 22k	External	44100	Digital
	DIG_ZONE_COAX1_IN_44K_TO_ANLG_ZONE_VAR_OUT																	
174	DIG_ZONE_COAX1_IN_44K_TO_ANLG_ZONE_VAR_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+3.83	+4.025	+3.590	40kHz LP	100k	<10 - >500k	External	44100	Digital
175	DIG_ZONE_COAX1_IN_44K_TO_ANLG_ZONE_VAR_OUT_FREQ	-1.00dBFS	-1.00dBFS	10-20k/40k	n/a	n/a	n/a	dBr	Level	<-0.07/-0.39	+0.10	-0.25/-0.75	None	100k	<10 - >500k	External	44100	Digital
176	DIG_ZONE_COAX1_IN_44K_TO_ANLG_ZONE_VAR_OUT_THD	-1.00dBFS	-1.00dBFS	20-1k/5k-8k/10k-40k	n/a	n/a	n/a	%	THD+N	<.002/.009/.025	.005/.010/.030	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital
177	DIG_ZONE_COAX1_IN_44K_TO_ANLG_ZONE_VAR_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-108.00	-105.00	-140.00	None	100k	<10 - 22k	External		Digital
	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_VAR_OUT_AADIRMUX																	
178	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_VAR_OUT_AADIRMUX	OFF *	OFF *	997	20	Unbal	Float	Vrms	Level	>-78.00	-72.00	-140.00	40kHz LP	100k	<10 - >500k	External	96000	Digital
	** AADIRMUX = Analog Zone Inputs are driven at 4.0Vrms with only the Digital Zone Input selected.*																	
	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT																	
179	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	96000	Digital
180	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_FREQ	-1.00dBFS	-1.00dBFS	10-20k/40k	n/a	n/a	n/a	dBr	Level	<-0.07/-0.54	+0.10	-0.25/-0.75	None	100k	<10 - >500k	External	96000	Digital
181	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	20-1k/5k-8k/10k-40k	n/a	n/a	n/a	%	THD+N	<.002/.009/.025	.003/.010/.030	.0002	40kHz LP	100k	<10 - >500k	External	96000	Digital
182	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_XTALK	-1.00dBFS	-1.00dBFS	15k	n/a	n/a	n/a	dB	Level	>-90.00	-80.00	-150.00	None	100k	<10 - 22k	External	96000	Digital
183	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-108.00	-140.00	40kHz LP	100k	<10 - 22k	External	96000	Digital
	DIG_MAIN_COAX2_IN_88K_TO_ANLG_MAIN_OUT																	
184	DIG_MAIN_COAX2_IN_88K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	88000	Digital
185	DIG_MAIN_COAX2_IN_88K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	88000	Digital
186	DIG_MAIN_COAX2_IN_88K_TO_ANLG_MAIN_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-108.00	-140.00	40kHz LP	100k	<10 - 22k	External	88000	Digital
	DIG_MAIN_COAX3_IN_48K_TO_ANLG_MAIN_OUT																	
187	DIG_MAIN_COAX3_IN_48K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	48000	Digital
188	DIG_MAIN_COAX3_IN_48K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	48000	Digital
189	DIG_MAIN_COAX3_IN_48K_TO_ANLG_MAIN_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-108.00	-140.00	40kHz LP	100k	<10 - 22k	External	48000	Digital
	DIG_MAIN_COAX4_IN_44K_TO_ANLG_MAIN_OUT																	
190	DIG_MAIN_COAX4_IN_44K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	44100	Digital
191	DIG_MAIN_COAX4_IN_44K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital
192	DIG_MAIN_COAX4_IN_44K_TO_ANLG_MAIN_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-108.00	-140.00	40kHz LP	100k	<10 - 22k	External	44100	Digital
	DIG_MAIN_COAX5_IN_44K_TO_ANLG_MAIN_OUT																	
193	DIG_MAIN_COAX5_IN_44K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	44100	Digital
194	DIG_MAIN_COAX5_IN_44K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital
	DIG_MAIN_COAX6_IN_44K_TO_ANLG_MAIN_OUT																	
195	DIG_MAIN_COAX6_IN_44K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	44100	Digital
196	DIG_MAIN_COAX6_IN_44K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital

	D-A Tests	Digital Generator Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Analog Analyzer Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	Clock Source	Sample Rate	Audio Source
	Test Name																	
	DIG_MAIN_COAX6_IN_44K_TO_ANLG_MAIN_OUT_AADIRMUX																	
197	DIG_MAIN_COAX6_IN_44K_TO_ANLG_MAIN_OUT_AADIRMUX	OFF **	OFF **	997	20	Unbal	Float	Vrms	Level	>-90.00	-80.00	-140.00	10-40k	100k	<10 - >500k	External	44100	Digital
	*** AADIRMUX = Analog Zone Inputs are driven at 4.0Vrms with only the Digital Zone Input selected.*																	
	DIG_MAIN_OPT1_IN_44K_TO_ANLG_MAIN_OUT																	
198	DIG_MAIN_OPT1_IN_44K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	44100	Digital
199	DIG_MAIN_OPT1_IN_44K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital
	DIG_MAIN_OPT2_IN_44K_TO_ANLG_MAIN_OUT																	
200	DIG_MAIN_OPT2_IN_44K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	44100	Digital
201	DIG_MAIN_OPT2_IN_44K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital
	DIG_MAIN_OPT3_IN_44K_TO_ANLG_MAIN_OUT																	
202	DIG_MAIN_OPT3_IN_44K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	44100	Digital
203	DIG_MAIN_OPT3_IN_44K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital
	DIG_MAIN_OPT4_IN_44K_TO_ANLG_MAIN_OUT																	
204	DIG_MAIN_OPT4_IN_44K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	44100	Digital
205	DIG_MAIN_OPT4_IN_44K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital
	DIG_MAIN_OPT5_IN_44K_TO_ANLG_MAIN_OUT																	
206	DIG_MAIN_OPT5_IN_44K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	44100	Digital
207	DIG_MAIN_OPT5_IN_44K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital
	DIG_MAIN_OPT6_IN_44K_TO_ANLG_MAIN_OUT																	
208	DIG_MAIN_OPT6_IN_44K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	44100	Digital
209	DIG_MAIN_OPT6_IN_44K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	44100	Digital
	DIG_MAIN_AES_IN_96K_TO_ANLG_MAIN_OUT																	
210	DIG_MAIN_AES_IN_96K_TO_ANLG_MAIN_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	96000	Digital
211	DIG_MAIN_AES_IN_96K_TO_ANLG_MAIN_OUT_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	96000	Digital
212	DIG_MAIN_AES_IN_96K_TO_ANLG_MAIN_OUT_CLKRNG	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	>-95.00	-90.00	-120.00	None	100k	<10 - 22k	External	97K-95K	Digital
	**** AP Switcher channels are selected during AP macro.*																	

	D-A XLR Tests *(MC12B ONLY)*	Digital Generator Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Analog Analyzer Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	Clock Source	Sample Rate	Audio Source
	Test Name																	
	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_VAR_OUT																	
215	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_VAR_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+7.75	+8.52	+7.05	40kHz LP	100k	<10 - >500k	External	96000	Digital
216	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_VAR_OUT_FREQ	-1.00dBFS	-1.00dBFS	10-20k/40k	n/a	n/a	n/a	dBr	Level	<-0.07/-0.39	+0.10	-0.25/-0.75	None	100k	<10 - >500k	External	96000	Digital
217	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_VAR_OUT_THD	-1.00dBFS	-1.00dBFS	20-1k/5k-40k	n/a	n/a	n/a	%	THD+N	<.005/.008	.005/.020	.0002	40kHz LP	100k	<10 - >500k	External	96000	Digital
218	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_VAR_OUT_XTALK	-1.00dBFS	-1.00dBFS	15k	n/a	n/a	n/a	dB	Level	>-78.00	-72.00	-150.00	None	100k	<10 - 22k	External	96000	Digital
219	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_VAR_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-105.00	-140.00	None	100k	<10 - 22k	External	96000	Digital
	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_VAR_OUT_600																	
220	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_VAR_OUT_GAIN_600	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+7.10	+7.80	+6.40	40kHz LP	100k	<10 - >500k	External	96000	Digital
221	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_VAR_OUT_THD_600	-1.00dBFS	-1.00dBFS	100	n/a	n/a	n/a	%	THD+N	<.005	.005	.0002	40kHz LP	100k	<10 - >500k	External	96000	Digital
	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_VAR_OUT_RELAY_MUTE																	
221	DIG_ZONE_COAX1_IN_96K_TO_ANLG_ZONE_XLR_VAR_OUT_RELAY_MUTE	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	-999.00	-75.00	-1001.00	40kHz LP	100k	<10 - >500k	External	96000	Digital
	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_FIX_OUT																	
222	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_FIX_OUT_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+16.00	+17.53	+14.51	40kHz LP	100k	<10 - >500k	External	96000	Digital
223	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_FIX_OUT_FREQ	-1.00dBFS	-1.00dBFS	10-20k/40k	n/a	n/a	n/a	dBr	Level	<-0.10/-0.50	+0.10	-0.25/-0.75	None	100k	<10 - >500k	External	96000	Digital
224	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_FIX_OUT_THD	-1.00dBFS	-1.00dBFS	20-1k/5k-40k	n/a	n/a	n/a	%	THD+N	<.002/.008	.003/.020	.0002	40kHz LP	100k	<10 - >500k	External	96000	Digital
225	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_FIX_OUT_XTALK	-1.00dBFS	-1.00dBFS	15k	n/a	n/a	n/a	dB	Level	>-78.00	-72.00	-150.00	None	100k	<10 - 22k	External	96000	Digital
226	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_FIX_OUT_DYNRNG	-60.00dBFS	-60.00dBFS	997	n/a	n/a	n/a	dBr	THD+N	>-110.00	-108.00	-140.00	None	100k	<10 - 22k	External	96000	Digital
	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_FIX_OUT_600																	
227	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_FIX_OUT_GAIN_600	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+14.70	+16.15	+13.37	40kHz LP	100k	<10 - >500k	External	96000	Digital
228	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_FIX_OUT_THD_600	-1.00dBFS	-1.00dBFS	100	n/a	n/a	n/a	%	THD+N	<.002	.005	.0002	40kHz LP	100k	<10 - >500k	External	96000	Digital
	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_FIX_OUT_RELAY_MUTE																	
229	DIG_MAIN_COAX1_IN_96K_TO_ANLG_MAIN_XLR_FIX_OUT_RELAY_MUTE	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	-999.00	-75.00	-1001.00	40kHz LP	100k	<10 - >500k	External	96000	Digital
	**** AP Switcher channels are selected during the AP macro.*																	

	D-A Tests	Digital Generator						Analog Analyzer										
	Test Name	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	Clock Source	Sample Rate	Audio Source
	DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT_DSP																	
213	DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT_DSP_GAIN	+0.00dBFS	+0.00dBFS	997	n/a	n/a	n/a	Vrms	Level	+8.13	+8.83	+7.43	40kHz LP	100k	<10 - >500k	External	96000	Digital
214	DIG_MAIN_OPT1_IN_96K_TO_ANLG_MAIN_OUT_DSP_THD	-1.00dBFS	-1.00dBFS	997	n/a	n/a	n/a	%	THD+N	<.002	.003	.0002	40kHz LP	100k	<10 - >500k	External	96000	Digital
	**** AP Switcher channels are selected during AP macro.*																	

	A-A Tests	Analog Generator						Analog Analyzer										
	Test Name	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	Clock Source	Sample Rate	Audio Source
	ANLG_REC_IN1_96K_TO_ANLG_REC_VAR_OUT																	
230	ANLG_REC_IN1_96K_TO_ANLG_REC_VAR_OUT_GAIN	4.00 Vrms	4.00 Vrms	997	20	Unbal	Float	Vrms	Level	+3.58	+3.71	+3.45	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
231	ANLG_REC_IN1_96K_TO_ANLG_REC_VAR_OUT_FREQ	2.00 Vrms	2.00 Vrms	10-20k/40k	20	Unbal	Float	dBr	Level	<-0.10/-0.50	+0.10	-0.25/-0.75	None	100k	<10 - >500k	Internal	96000	Analog
232	ANLG_REC_IN1_96K_TO_ANLG_REC_VAR_OUT_THD	4.0Vrms	4.0Vrms	20-8k/10k-40k	20	Unbal	Float	%	THD+N	<.025/.002	.015/.03	.00005	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
233	ANLG_REC_IN1_96K_TO_ANLG_REC_VAR_OUT_XTALK	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-85.00	-75.00	150.00	None	100k	<10 - >22k	Internal	96000	Analog
234	ANLG_REC_IN1_96K_TO_ANLG_REC_VAR_OUT_SNR	OFF	OFF	997	20	Unbal	Float	dBr	Level	-101.00	-98.00	-140.00	None	100k	<10 - >22k	Internal	96000	Analog
235	ANLG_REC_IN1_96K_TO_ANLG_REC_VAR_OUT_OUTLEVEL_MUTE	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	>-103.00	-90.00	-1001.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
236	ANLG_REC_IN1_96K_TO_ANLG_REC_VAR_OUT_DADIRMUX	OFF ***	OFF ***	997	20	Unbal	Float	Vrms	Level	>-101.00	-90.00	-140.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
237	ANLG_REC_IN1_96K_TO_ANLG_REC_VAR_OUT_RELAY_MUTE	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	-999.00	-90.00	-1001.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
	ANLG_REC_IN1_96K_TO_ANLG_REC_FIX_OUT																	
238	ANLG_REC_IN1_96K_TO_ANLG_REC_FIX_OUT_RELAY_MUTE	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	-999.00	-90.00	-1001.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
	ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_VAR_OUT																	
239	ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_VAR_OUT_GAIN	4.00 Vrms	4.00 Vrms	997	20	Unbal	Float	Vrms	Level	+3.58	+3.71	+3.45	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
240	ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_VAR_OUT_FREQ	2.00 Vrms	2.00 Vrms	10-20k/40k	20	Unbal	Float	dBr	Level	<-0.10/-0.50	+0.10	-0.25/-0.75	None	100k	<10 - >500k	Internal	96000	Analog
241	ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_VAR_OUT_THD	4.0Vrms	4.0Vrms	20-8k/10k-40k	20	Unbal	Float	%	THD+N	<.025/.002	.015/.03	.00005	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
242	ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_VAR_OUT_XTALK	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-85.00	-75.00	150.00	None	100k	<10 - >22k	Internal	96000	Analog
243	ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_VAR_OUT_SNR	OFF	OFF	997	20	Unbal	Float	dBr	Level	-101.00	-98.00	-140.00	None	100k	<10 - >22k	Internal	96000	Analog
244	ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_VAR_OUT_OUTLEVEL_MUTE	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	>-103.00	-90.00	-1001.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
245	ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_VAR_OUT_DADIRMUX	OFF ***	OFF ***	997	20	Unbal	Float	Vrms	Level	>-101.00	-90.00	-140.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
246	ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_VAR_OUT_RELAY_MUTE	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	-999.00	-90.00	-1001.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
	ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_FIX_OUT																	
247	ANLG_ZONE_IN1_96K_TO_ANLG_ZONE_FIX_OUT_RELAY_MUTE	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	-999.00	-90.00	-1001.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT																	
248	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT_GAIN	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	+7.50	+8.40	+6.60	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
249	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT_FREQ	2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.60/-0.15	+0.10	-0.30/-0.80	None	100k	<10 - >500k	Internal	96000	Analog
250	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT_THD	4.0Vrms	4.0Vrms	20-1k/5-40k	20	Unbal	Float	%	THD+N	<.007/.013	.01/.02	.00005	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
251	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT_XTALK	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-85.00	-75.00	150.00	None	100k	<10 - >22k	Internal	96000	Analog
252	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT_SNR	OFF	OFF	997	20	Unbal	Float	dBr	Level	-103.00	-100.00	-140.00	None	100k	<10 - >22k	Internal	96000	Analog
253	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT_OUTLEVEL_MUTE	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	>-110.00	-100.00	1001.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
254	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_OUT_RELAY_MUTE	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	>-999.00	-90.00	1001.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_DIR_OUT																	
255	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_DIR_OUT_GAIN	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	+8.00	+8.00	+7.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
256	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_DIR_OUT_FREQ	2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25	None	100k	<10 - >500k	Internal	96000	Analog
257	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_DIR_OUT_THD	4.0Vrms	4.0Vrms	20-1k/5-40k	20	Unbal	Float	%	THD+N	<.007/.013	.01/.02	.00005	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
258	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_DIR_OUT_SNR	OFF	OFF	997	20	Unbal	Float	dBr	Level	-103.00	-100.00	-140.00	None	100k	<10 - >22k	Internal	96000	Analog
259	ANLG_MAIN_IN1_96K_TO_ANLG_MAIN_DIR_OUT_DADIRMUX	OFF ***	OFF ***	997	20	Unbal	Float	Vrms	Level	>-101.00	-90.00	-140.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
	ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_DIR_OUT																	
260	ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_DIR_OUT_GAIN	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	+8.00	+8.50	+7.50	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
261	ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_DIR_OUT_FREQ	2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25	None	100k	<10 - >500k	Internal	96000	Analog
262	ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_DIR_OUT_THD	4.0Vrms	4.0Vrms	20-1k/5-40k	20	Unbal	Float	%	THD+N	<.007/.013	.01/.02	.00005	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
263	ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_DIR_OUT_XTALK	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-90.00	-75.00	150.00	None	100k	<10 - >22k	Internal	96000	Analog
264	ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_DIR_OUT_SNR	OFF	OFF	997	20	Unbal	Float	dBr	Level	-103.00	-100.00	-140.00	None	100k	<10 - >22k	Internal	96000	Analog
265	ANLG_MAIN_IN7_96K_TO_ANLG_MAIN_DIR_OUT_DADIRMUX	OFF ***	OFF ***	997	20	Unbal	Float	Vrms	Level	>-101.00	-90.00	-140.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
	ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_DIR_OUT																	
266	ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_DIR_OUT_GAIN	4.0Vrms	4.0Vrms	997	20	Unbal	Float	Vrms	Level	+8.00	+8.50	+7.50	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
267	ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_DIR_OUT_FREQ	2.00 Vrms	2.00 Vrms	10-40k	20	Unbal	Float	dBr	Level	<-0.10	+0.10	-0.25	None	100k	<10 - >500k	Internal	96000	Analog
268	ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_DIR_OUT_THD	4.0Vrms	4.0Vrms	20-1k/5-40k	20	Unbal	Float	%	THD+N	<.007/.013	.01/.02	.00005	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
269	ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_DIR_OUT_XTALK	4.0Vrms	4.0Vrms	15k	20	Unbal	Float	dB	Level	>-90.00	-75.00	150.00	None	100k	<10 - >22k	Internal	96000	Analog
270	ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_DIR_OUT_SNR	OFF	OFF	997	20	Unbal	Float	dBr	Level	-103.00	-100.00	-140.00	None	100k	<10 - >22k	Internal	96000	Analog
271	ANLG_MAIN_IN8_96K_TO_ANLG_MAIN_DIR_OUT_DADIRMUX	OFF ***	OFF ***	997	20	Unbal	Float	Vrms	Level	>-101.00	-90.00	-140.00	40kHz LP	100k	<10 - >500k	Internal	96000	Analog
	**** Switcher channels are selected during AP macro.*																	
	***** Digital Inputs are driven at -1dBFS*																	

	D-D Tests	Analog Generator						Analog Analyzer										
	Test Name	Left	Right	Freq (Hz)	Z-out	Bal/ Unbal	Gnd/ Float	Level	Measure	Typical Reading	Upper Limit	Lower Limit	Filter	Imp.	Band.	Clock Source	Sample Rate	Audio Source
	DIG_REC_OPT1_IN_96K_TO_DIG_REC_OPT_OUT																	
280	DIG_REC_OPT1_IN_96K_TO_DIG_REC_OPT_OUT_GAIN	-1dBFS	-1dBFS	997	n/a	n/a	n/a	dBFS	Level	-0.999	-0.90	-1.10	n/a	n/a	<10 - Fs/2	External	96000	Analog
281	DIG_REC_OPT1_IN_96K_TO_DIG_REC_OPT_OUT_THD	-1dBFS	-1dBFS	10-40k	n/a	n/a	n/a	dBFS	THD+N	-144.00	-140.00	-999.00	n/a	n/a	<10Hz->20kHz LP	External	96000	Analog
	DIG_REC_OPT1_IN_96K_TO_DIG_REC_OPT_OUT_44K																	
283	DIG_REC_OPT1_IN_96K_TO_DIG_REC_OPT_OUT_44K_GAIN	-1dBFS	-1dBFS	997	n/a	n/a	n/a	dBFS	Level	-1.067	-0.90	-1.20	n/a	n/a	<10 - Fs/2	External	96000	Analog
284	DIG_REC_OPT1_IN_96K_TO_DIG_REC_OPT_OUT_44K_THD	-1dBFS	-1dBFS	10-40k	n/a	n/a	n/a	dBFS	THD+N	-127.00	-110.00	-999.00	n/a	n/a	<10Hz->20kHz LP	External	96000	Analog
	DIG_REC_OPT1_IN_44K_TO_DIG_REC_OPT_OUT_96K																	
286	DIG_REC_OPT1_IN_44K_TO_DIG_REC_OPT_OUT_96K_GAIN	-1dBFS	-1dBFS	997	n/a	n/a	n/a	dBFS	Level	-1.066	-0.90	-1.20	n/a	n/a	<10 - Fs/2	External	44100	Analog
287	DIG_REC_OPT1_IN_44K_TO_DIG_REC_OPT_OUT_96K_THD	-1dBFS	-1dBFS	10-40k	n/a	n/a	n/a	dBFS	THD+N	-117.00	-110.00	-999.00	n/a	n/a	<10Hz->20kHz LP	External	44100	Analog

Chapter 5 Troubleshooting

Check the Lexicon web site for the latest software and information:
http://www.lexicon.com

The Lexicon Support Knowledgebase:
http://www.lexicon.com/kbase/index.asp

V1.00 Release Notes

The following are additions and modifications to the MC-12/MC-12 Balanced User Guide (Rev 1) based on Software
Version 1.0 (*note - page numbers refer to the User Guide, not this Service Manual)*:

1. The Mute LED lights whenever mute is activated either manually or automatically by the unit. For example, the unit will briefly activate mute when changing input types or listening modes. (Page 2-3)
2. When using an analog input source, the ZONE 2 AUDIO OUTPUTS and RECORD AUDIO OUTPUTS are approximately 2dB higher than the MAIN AUDIO OUTPUTS labeled FRONT L/R. When using a digital input source, the ZONE 2 AUDIO OUTPUTS and RECORD AUDIO OUTPUTS are approximately 8dB higher than the MAIN AUDIO OUTPUTS labeled FRONT L/R. This is to accommodate THX level requirements. (Page 2-5)
3. When the 2-CH parameter on the INPUT SETUP menu is set to USE LAST, pressing the 2CH button on the remote control selects the 2-CHANNEL listening mode. However, pressing the 2CH button again does not select the previous listening mode. To deselect the 2-CHANNEL listening mode, press another mode family selection button or reselect the input. (Pages 2-14 and 3-10)
4. Zone 2 and the Record Zone will provide a downmix (a 2-channel version of multi-channel digital audio) only when using the same input that is selected in the Main Zone. (Page 2-16)
5. Audio will mute for up to 2 seconds when: The same input is selected in the Main Zone that is already selected in Zone 2 or the Record Zone. Likewise, when the input is deselected in the Main Zone. The same input is selected in Zone 2 or the Record Zone that is already selected in the Main Zone. Likewise, when the input is deselected in Zone 2 or the Record Zone. (Page 2-16)
6. When a connector is selected for both the DIGITAL IN and ANALOG IN parameters, all INPUT SELECT parameters will automatically be set to AUTO. The DIGITAL IN and ANALOG IN parameters are located on the INPUT SETUP menu. The INPUT SELECT parameters are located on the MAIN ADV, ZONE 2 ADV, and RECORD ADV menus. (Pages 3-5, 3-6, 3-13, 3-15, and 3-16)
7. The level meters on the ANLG IN LVL menu indicate signal levels for the selected input, whether the input signal is analog or digital. For example, if the input signal is digital only, the level meters will indicate the digital input signal levels. (Page 3-6)
8. The factory-default setting of the COMPONENT OSD parameter is OFF. When set to ON, the component on-screen display appears on a full blue-screen background. This includes the two-line status. The COMPONENT OSD parameter is located on the MAIN ADV menu. (Page 3-14)
9. The ANLG IN LVL parameter on the RECORD ADV menu only affects the digital RECORD AUDIO OUTPUT labeled S/PDIF. This is used to prevent the internal analog-to-digital converter from overloading. This can be adjusted while listening to an input source. (Page 3-17)
10. Changing the setting of the DIG OUT RATE parameter will cause the digital RECORD AUDIO OUTPUT labeled S/PDIF to mute momentarily, even if the DIGITAL BYPASS parameter is set to ON. The DIG OUT RATE and DIGITAL BYPASS parameters are located on the RECORD ADV menu. (Page 3-17)
11. When the REAR L/R parameter is set to NONE, the unit redirects rear channel signals to the SIDE L/R outputs. This item refers to the REAR L/R parameter on the CUSTOM SETUP menu. (Page 3-21)
12. Speaker parameters that are set to NONE or OFF on the CUSTOM SETUP menu cannot be adjusted during the INTERNAL NOISE TEST. These speakers can be adjusted during the EXTERNAL NOISE TEST or on the SPEAKER DISTANCES menu, but this is not recommended. (Pages 3-18 to 3-23, and 3-26 to 3-27)
13. The INTERNAL NOISE TEST calibration noise will pass briefly through the SUB R output when:
    13.1. The SUB L/R parameter on the CUSTOM SETUP or THX SETUP menus is set to MONO. (Pages 3-22 and 3-24)

13.2. During the INTERNAL NOISE TEST, the SUB RIGHT parameter on the SPEAKER LEVELS ADJUST menu is manually selected. (Page 3-26)

14. During the INTERNAL NOISE TEST, it is possible to manually select a speaker just as the unit is about to automatically scroll to the next speaker. This may cause the unit to send the noise signal to both outputs. If this occurs, reselect the desired speaker. (Page 3-26)
15. Selecting EXTERNAL NOISE TEST on the LEVELS CALIBRATION menu will mute audio when the unit is configured for analog bypass. To restore audio, exit the SPEAKER LEVELS ADJUST menu. To deactivate analog bypass, set the ANALOG BYPASS parameter on the MAIN ADV menu to OFF (page 3-13). (Pages 3-26 and 3-27)
16. When the SETUP parameter is set to LOCKED, the STATUS parameter on the ON-SCREEN DISPLAY and FRONT PANEL DISPLAY menus can still be set using the FP, BLUE, and OSD buttons on the remote control. The SETUP parameter is located on the LOCKED OPTIONS menu. (Page 3-36)
17. The MONO listening mode includes a SUB L/R parameter. (Page 5-7)
18. When a THX speaker configuration is selected, the LFE parameter will appear on the OUTPUT LEVELS menu for the 5.1 THX SURROUND EX or 5.1 THX and dts(-ES) THX listening modes. This parameter only has an effect when the LFE parameter on the CUSTOM SETUP menu is set to ON (page 3-23). (Pages 5-10 and 5-14)
19. The 5.1 MONO, 5.1 MONO LOGIC, and 5.1 MONO SURR listening modes are designed for playback of Dolby Digital mono sources. Mono material can be found on both Dolby Digital 1.0 and 2.0 input types. These modes are also available, but not recommended, for 5.1 Dolby Digital sources. The unit will automatically select 5.1 MONO LOGIC when a 1.0 Dolby Digital input type is present. (Pages 5-12 to 5-13)
20. It is possible to scroll through STATUS menu parameters with the MENU arrows for front panel display viewing. STATUS menu parameters are not adjustable. (Page 5-18)
21. Toggling the setting of the SURROUND EX parameter produces low-level clicks in the front speakers. Pressing the THX button on the remote control when the SHIFT command bank is active will still toggle the SURROUND EX parameter setting when the MODES parameter on the LOCK OPTIONS menu is set to LOCKED (page 3-36). Pressing the 7/5 button on the remote control will not toggle the SURROUND EX parameter setting when either the REAR L/R or SIDE L/R parameters are set to NONE. The REAR L/R and SIDE L/R parameters are located on the CUSTOM SETUP and THX SETUP menus (pages 3-21 and 3-24). (Page 5-24)
22. The THD + Noise specification for the Main Zone, Zone 2, and the Record Zone is: “Below .008% at 1kHz, maximum output level.” (Page A-2)
23. The MC-12/MC-12/MC-12 Balanced Balanced does not support MPEG input types.
24. Some DVD players will produce audio artifacts when switching audio formats.

Diagnostics

INTRODUCTION

This section contains a complete description of the diagnostic tests for the MC-12/MC-12 Balanced. The diagnostics in the MC-12/MC-12 Balanced are used to verify functionality of the unit and to aid in troubleshooting defective units.

DIAGNOSTICS CATEGORIES

There are 2 types of diagnostics in the MC-12/MC-12 Balanced, power-on and extended. The extended diagnostics contain the tests that are used by Lexicon manufacturing personnel to verify functionality and by repair personnel to aid in troubleshooting. The entire set of power-on diagnostics is executed every time a unit is powered on using the rear panel power switch. The power-on diagnostic tests can be run individually in the extended diagnostics. The extended diagnostics also contain additional tests used to verify all the front panel controls, infrared communications, audio and video performance, etc. The troubleshooting or repair diagnostics are utilized to troubleshoot an MC-12/MC-12 Balanced if any test fails.

POWER-ON MODES

There are two power-on modes available via the rear panel power switch or by bringing the MC-12/MC-12 Balanced out of standby mode. The power-on diagnostics are executed every time the rear panel power switch is switched on. When an MC-12/MC-12 Balanced is operating, if the front panel Standby button is pressed, the unit goes into a low-power/standby mode. Pressing any front panel button or any remote key will bring the MC-12/MC-12 Balanced out of low-power/standby mode. No diagnostics are run when the unit is brought out of standby.

DIAGNOSTICS REPORTING

All diagnostic functionality is reported to the VFD (Vacuum Fluorescent Display), and to the front panel LEDs. They report on what test is being executed, and if the test passed or failed. The LEDs are utilized to report diagnostic status in the event that the VFD is not functioning.

Diagnostic status and data is also available on an external PC or a terminal, via the serial debug port located at the D9 connector labeled RS232 2 on the rear panel of the MC-12/MC-12 Balanced. The D9 connector labeled RS232 1 is used for updating the flash memory. In the event a diagnostic failure occurs, additional failure information, such as data sent, data received, address location, etc., is listed in the error log. The error log can be viewed either via the VFD, or it can be sent to the serial debug port.

VFD (Vacuum Fluorescent Display)

The VFD is the primary source of information during diagnostics. The exact display information will depend on the test or tests being executed. When an individual diagnostic test is executed, the VFD will display the name of that test. Groups of tests, such as during power-on diagnostics or the burn-in loop, have a generic message on the top line of the VFD. For example DIAGNOSTIC TESTS is on the VFD while the power-on diagnostics is being run. Failure messages are displayed by an E followed by a number that indicates which test failed.

Front Panel LEDs

The top row of the front panel LEDs are also used to display diagnostic status. The LEDs are used in binary format with the Record LD LED as the LSB and the Main DVD 1 LED as the MSB. Running test number 1 would illuminate the Record LD LED only with all the others off. Running test number 2 would illuminate the Record DVD 2 LED only with all others off. Running test number 3 would illuminate the Record LD and the Record DVD 2 LEDs together with all others off, etc. The table below lists the tests run and what front panel LEDs are used to indicate them. Not all of the tests listed are performed during power-on. Those tests that are run during power-on are listed in the "In Use" column with a '+'. Those marked with a '-' are not. The table shows all of the tests available, not just power-on tests.

Test Num	Test Name	In Use	Front Panel LEDs On
1	Trap Opcode	+	Blink Standby LED 1 time/interval
2	EPROM Chksum Via EPROM	+	Blink Standby LED 2 times/interval
3	Z180 SRAM	+	Blink Standby LED 3 times/interval
4	Flash Checksum Via EPROM	+	Blink Standby LED 4 times/interval
5	VFD Memory	+	Rec. DVD 1 and Record LD
6	IO FPGA	+	Rec. DVD 1 and Record DVD 2
7	Digital Audio Receiver FPGA	+	Rec. DVD 1 and Rec. DVD 2 and Record LD
8	Audio FPGA	+	Z2 LD
9	Analog FPGA	+	Z2 LD and Rec. LD
10	Crystal 49326 Boot Test	+	Z2 LD and Rec. DVD 2
11	Crystal 8420 Version Id Test	+	Z2 LD and DVD 2 and Rec. LD
12	SHARC Pair 0 PS1 GPIO	-	Z2 LD and Rec. DVD 1
13	SHARC Pair 0 PS2 GPIO	-	Z2 LD and Rec. DVD 1 and Rec. LD
14	SHARC Pair 1 PS1 GPIO	-	Z2 LD and Rec. DVD 1 and Rec. DVD2

15	SHARC Pair 1 PS2 GPIO	-	Z2 LD and Rec. DVD1 and Rec. DVD2 and LD
16	SHARC Pair 0 PS1 SDRAM Test	+	Z2 DVD1
17	SHARC Pair 0 PS2 SDRAM Test	-	Z2 DVD2 and Rec. LD
18	SHARC Pair 1 PS1 SDRAM Test	+	Z2 DVD2 and Rec. DVD2
19	SHARC Pair 1 PS2 SDRAM Test	-	Z2 DVD2 and Rec. DVD2 and Rec. LD
20	SHARC Pair 0 PS1 SRAM Test	-	Z2 DVD2 and Rec. DVD1
21	SHARC Pair 0 PS2 SRAM Test	+	Z2 DVD2 and Rec. DVD1 and Rec. LD
22	SHARC Pair 1 PS1 SRAM Test	-	Z2 DVD2 and Rec. DVD1and Rec. DVD2
23	SHARC Pair 1 PS2 SRAM Test	+	Z2 DVD2 and Rec. DVD1 and Rec. DVD2 and Rec. LD
24	SHARC Pair 0 Boot	-	Z2 DVD2 and Z2 LD
25	SHARC Pair 1 Boot	-	Z2 DVD2 and Z2 LD and Rec. LD
26	SHARC Pair 2 Boot	-	Z2 DVD2 and Z2 LD and Rec. DVD2
27	SHARC Pair 3 Boot	-	Z2 DVD2 and Z2 LD and Rec. DVD2 and Rec. LD
28	EPROM Chksum Via Flash	-	Z2 DVD2 and Z2 LD and Rec. DVD1
29	FLASH Chksum Via Flash	-	Z2 DVD2 and Z2 LD and Rec. DVD1 and Rec. LD
30	RS232 Wrap Test	-	Z2 DVD2 and Z2 LD and Rec. DVD1 and Rec. DVD2
31	ID Remote Test	-	Z2 DVD2 and Z2 LD and Rec. DVD1 and Rec. DVD2 and Rec. LD
32	VFD Char Test	-	Z2 DVD1
33	VFD Block Test	-	Z2 DVD1 and Rec. LD
34	OSD Char Test	-	Z2 DVD1and Rec. DVD2
35	Switch Test	-	Z2 DVD1 and Rec. DVD2 and Rec. LD
36	LED Test	-	Z2 DVD1 and Rec. DVD1
37	View ERRORLOG	-	Z2 DVD1 and Rec. DVD1 and Rec. LD
38	Clear NON-VOL SRAM	-	Z2 DVD1 and Rec. DVD1 and Rec.DVD2
39	Normal Operation	-	Z2 DVD1 and Rec. DVD1 and Rec. DVD2 and Rec. LD
40	Manufacturing Tests Start	-	Z2 DVD1 and Z2 LD
41	Pre-Burn Tests Start	-	Z2 DVD1 and Z2 LD and Rec. LD
42	Burn-In Tests Start	-	Z2 DVD1 and Z2 LD and Rec. DVD2
43	SHARC Pair 2 PS1 GPIO	-	Z2 DVD1 and Z2 LD and Rec. DVD2 and Rec. LD
44	SHARC Pair 2 PS2 GPIO	-	Z2 DVD1 and Z2 LD and Rec. DVD1
45	SHARC Pair 3 PS1 GPIO	-	Z2 DVD1 and Z2 LD and Rec. DVD1 and Rec. LD
46	SHARC Pair 3 PS2 GPIO	-	Z2 DVD1 and Z2 LD and Rec. DVD1 and Rec. DVD2
47	SHARC Pair 4 PS1 GPIO	-	Z2 DVD1 and Z2 LD and Rec. DVD1 and Rec. DVD2 and Rec. LD
48	SHARC Pair 4 PS2 GPIO	-	Z2 DVD1 and Z2 DVD2
49	SHARC Pair 5 PS1 GPIO	-	Z2 DVD1 and Z2 DVD2 and Rec. LD
50	SHARC Pair 5 PS2 GPIO	-	Z2 DVD1 and Z2 DVD2 and Rec. DVD2
51	SHARC Pair 6 PS1 GPIO	-	Z2 DVD1 and Z2 DVD2 and Rec. DVD2 and Rec. LD
52	SHARC Pair 6 PS2GPIO	-	Z2 DVD1 and Z2 DVD2 and Rec. DVD1
53	SHARC Pair 7 PS1 GPIO	-	Z2 DVD1 and Z2 DVD2 and Rec. DVD1 and Rec. LD
54	SHARC Pair 7 PS2 GPIO	-	Z2 DVD1 and Z2 DVD2 and Rec. DVD1 and Rec. DVD2
55	SHARC Pair 2 PS1 SDRAM	-	Z2 DVD1 and Z2 DVD2 and Rec. DVD1 and Rec. DVD1 and Rec. LD
56	SHARC Pair 2 PS2 SDRAM	-	Z2 DVD1 and Z2 DVD2 and Z2 LD
57	SHARC Pair 3 PS1 SDRAM	-	Z2 DVD1 and Z2 DVD2 and Z2 LD and Rec. LD
58	SHARC Pair 3 PS2 SDRAM	-	Z2 DVD1 and Z2 DVD2 and Z2 LD and DVD2
59	SHARC Pair 4 PS1 SDRAM	-	Z2 DVD1 and Z2 DVD2 and Z2 LD and Rec. DVD2 and Rec. LD
60	SHARC Pair 4 PS2 SDRAM	-	Z2 DVD1 and Z2 DVD2 and Z2 LD and Rec. DVD1

61	SHARC Pair 5 PS1 SDRAM	-	Z2 DVD1 and Z2 DVD1 and Z2 LD and Rec. DVD1 and Rec. LD
62	SHARC Pair 5 PS2 SDRAM	-	Z2 DVD1 and Z2 DVD2 and Z2 LD and Rec. DVD1 and Rec. DVD2
63	SHARC Pair 6 PS1 SDRAM	-	Z2 DVD1 and Z2 DVD2 and Z2 LD and Rec. DVD1 and Rec. DVD2 and Rec. LD
64	SHARC Pair 6 PS2 SDRAM	-	Main LD
65	SHARC Pair 7 PS1 SDRAM	-	Main LD and Rec. LD
66	SHARC Pair 7 PS2 SDRAM	-	Main LD and Rec. DVD2
67	SHARC Pair 2 PS1 SRAM	-	Main LD and Rec. DVD2 and Rec. LD
68	SHARC Pair 2 PS2 SRAM	-	Main LD and Rec. DVD1
69	SHARC Pair 3 PS1 SRAM	-	Main LD and Rec. DVD1 and Rec. LD
70	SHARC Pair 3 PS2 SRAM	-	Main LD and Rec. DVD1 and Rec. DVD2
71	SHARC Pair 4 PS1 SRAM	-	Main LD and Rec. DVD1 and Rec. DVD2 and Rec. LD
72	SHARC Pair 4 PS2 SRAM	-	Main LD and Z2 LD
73	SHARC Pair 5 PS1 SRAM	-	Main LD and Z2 LD and Rec. LD
74	SHARC Pair 5 PS2 SRAM	-	Main LD and Z2 LD and Rec.DVD2
75	SHARC Pair 6 PS1 SRAM	-	Main LD and Z2 LD and Rec. DVD2 and Rec. LD
76	SHARC Pair 6 PS2 SRAM	-	Main LD and Z2 LD and Rec. DVD1
77	SHARC Pair 7 PS1 SRAM	-	Main LD and Z2 LD and Rec. DVD1 and Rec. LD
78	SHARC Pair 7 PS2 SRAM	-	Main LD and Z2 LD and Rec. DVD1 and Rec. DVD2
79	SHARC Pair 4 Boot	-	Main LD and Z2 LD and Rec. DVD1 and Rec. DVD2 and Rec. LD
80	SHARC Pair 5 Boot	-	Main LD and Z2 DVD1
81	SHARC Pair 6 Boot	-	Main LD and Z2 DVD1 and Rec. LD
82	SHARC Pair 7 Boot	-	Main LD and Z2 DVD1 and Rec. DVD2
83	Pre-burn SRAM		Main LD and Z2 DVD2 and Rec. DVD2 and Rec. LD
84	Burn-in Z180 SRAM		Main LD and Z2 DVD2 and Rec. DVD1

If a failure occurs, the MUTE LED is illuminated to indicate the test failure, and the LEDs indicating which test was running when the failure occurred will also continue to be illuminated. The diagnostics will attempt to continuously execute the failed test (a test loop) to keep the signal lines active as an aid in debugging the failure.

Serial Debug Port

The Serial Debug Port is available to provide diagnostic status to be viewed on an external PC from the D9 connector labeled RS232 2. Using a terminal or a PC running a terminal program connected to Remote 2, the progress of the diagnostics can be monitored and test failure information is reported. Also, the error log can be dumped to the serial debug port while in extended diagnostics. The serial protocol is 19,200bps, 8, N, 1, (8 data bits, no parity and 1 stop bit).

Error Log

An error log, or ring buffer, containing a log of the last 20 (13h) failures is available. If the error quantity exceeds 20, additional error messages are stored at the first location in the buffer (FIFO). The error log is stored in the non-volatile section of SRAM. Every failure stored in the error log has 6 parts:

#NN E## tXX aYYYYYY
wZZZZZZ rQQQQQQ

#NN: Error Log Number.

The error log location number, in hexadecimal. It goes from 00 to 13. Turning the ENCODER knob clockwise allows one to scroll through all 20 error log locations.

E##: Failure Number.

The E stands for error & the 2-digit number indicates which test failed.

tXX: Error Code from the following list

NO_ERROR	0
ADDR_FAILURE	1
DATA_FAILURE	2
TIMEOUT_FAILURE	3
COUNTER_FAILURE	4
NON_VOL_DATA_FAILURE	5
OPCODE_FAILURE	6
IO_FPGA_ID_NO_MATCH	7
DAR_FPGA_ID_NO_MATCH	8
AUDIO_FPGA_ID_NO_MATCH	9
ANALOG_FPGA_ID_NO_MATCH	0xA
VFD_TIME_OUT	0xB
VFD_RAM_ERROR	0xC
SRAM_PREBURNIN_FAILURE	0x13
SRAM_BURN_IN_FAILURE	0x14
EPROM_CHKSUM_FROM_FLASH	0x15
SRAM_FAILURE	0x16
FIFO_ERROR_OVERRUN	0x17
CS49326_NO_BOOT_START_MESSAGE	0x100
CS49326_NO_BOOT_SUCCESS_MESSAGE	0x101
CS49326_INIT_ERROR	0x102
CS49326_ISC_WR_TIMEOUT	0x103
CS49326_ISC_RD_TIMEOUT	0x104
CS49326_INTREQ_TIMEOUT	0x105
CS49326_AUTO_BOOT_FAILURE	0x106
CS8420_INIT_ERROR	0x200
CS8420_ISC_WR_TIMEOUT	0x201
CS8420_ISC_RD_TIMEOUT	0x202
CS8420_WRONG_VERSION	0x203
CS8420_WRONG_ID	0x204
SHARC_BAD_OPCODE	0x300
SHARC_TX_TIMEOUT	0x301
SHARC_RX_TIMEOUT	0x302
SHARC_GPIO_FAILURE	0x302
SHARC_SDRAM_FAILURE	0x304
SHARC_SRAM_FAILURE	0x305

aYYYYYY: Failing address location.

The address, in hexadecimal, where the failure occurred.

wZZZZZZ: Value Written.

The target value, in hexadecimal, that was written to the address where the failure occurred.

rQQQQQQ: Value Read.

The actual value, in hexadecimal, that was read from the address where the failure occurred.

The error log is available as a menu item in the extended diagnostics under Repair Tests. In addition, the error log can be viewed on an external PC or terminal via the D9 connector labeled RS232 2 on the rear panel of the MC-12/MC-12 Balanced. The error log is sent to RS232 2 when the VIEW ERRORLOG selection is made.

DIAGNOSTICS CONTROL/INTERFACE

Various combinations of button pushes are used to control diagnostic activity. During power-on diagnostics the following options are available:

Entering Diagnostics, RECORD LD & ZONE 2 LD

Pressing and holding the **RECORD LD** and **ZONE 2 LD** front panel buttons when powering on a MC-12/MC-12 Balanced will put the unit into the extended diagnostics. The extended diagnostics can also be entered via the serial debug port by first entering the debug program. Typing 'debug' when connected to the serial port accesses the debug program. The debug program is case sensitive. In addition the extended diagnostics can be entered by sending "ed", for extended diagnostics, to the unit via the serial debug port during the first 10 seconds after powering on the unit.

Skip Power-on Diagnostics, ZONE 2 AUX& RECORD AUX

Skip the power up diagnostics and go right to the operating system. Immediately after sufficient testing is performed to verify the system can boot (the Z180 CPU, EPROM, Z80 SRAM, FPGAs loaded, VFD etc.) after each subsequent test, the diagnostics check to see if the **ZONE 2 AUX** and **RECORD AUX** front panel buttons are being pressed together. If they are, the unit will attempt to skip the rest of the power up diagnostic tests and jump to the operating system.

Branch to Extended Diagnostics, RECORD OFF & ZONE 2 OFF

Pressing and holding the **RECORD OFF** and **ZONE 2 OFF** front panel buttons after a failure occurs will cause the unit to attempt to jump to the extended diagnostics. After a failure occurs the unit will attempt to display, on the VFD, and the front panel LEDs, the failed test number and loop on the failing test. If the Z180 CPU and support circuitry is not working the unit will not attempt to read any front panel switches.

Go to the Next Diagnostic Test, RECORD GAME & ZONE 2 GAME

Assuming the Z180 CPU and support circuitry is working, pressing and holding the **RECORD GAME** and **ZONE 2 GAME** front panel buttons after a failure occurs will cause the MC-12/MC-12 Balanced to attempt to execute the next power-on diagnostic step. If a failure occurs the MC-12/MC-12 Balanced attempts to enter a test loop to keep the signal lines active as an aid in debugging the failure. At the end of each successive loop, the diagnostics will check to see if the RECORD GAME and ZONE 2 GAME buttons are being held. Depending on the length of the test, the amount of time required to press and hold the buttons will vary.

POWER-ON DIAGNOSTICS

As described earlier there are two power-on modes in the MC-12/MC-12 Balanced . Power-on via the rear panel power switch and coming out of standby mode. Power-on diagnostics are executed every time the rear panel power switch is switched on. Diagnostics are not run when the unit is brought out of Standby.

Power-on diagnostics take approximately 40 seconds to complete. The power-on diagnostics are intended to verify basic hardware functionality of an MC-12/MC-12 Balanced. Additional diagnostic tests are available for manufacturing and customer service to completely test the hardware, and for debugging failures.

Initially, an attempt is made to illuminate the VFD and front panel LEDs for approximately five seconds. However during the first 6 tests/processes, the VFD will not be considered functional due to it not being tested. During these tests (Trap Op Code, EPROM, FLASH Checksum, Z80 SRAM, programming of FPGAs, and VFD RAM) the unit will attempt to use the STANDBY LED to indicate if a failure occurs. As soon as these are completed the VFD will display:

```
    DIAGNOSTIC TESTS
…                      …
```

The dots increment in number from both sides simultaneously, as the rest of the power-on diagnostic tests are completed. This informs the user that the unit is still functioning. The audio outputs (digital and analog) will be muted during this sequence.

The following is a list of test explanations. The front panel display is shown only for the first test that can use the VFD.

Trap Opcode

The Trap Opcode error occurs if during the initial boot sequence an undefined Opcode is fetched. The INT/TRAP Control register can be used to determine the starting address of the undefined instruction. If the trap error occurs an attempt will be made to blink the STANDBY LED using a rate of a single blink per several seconds, and the test will attempt to enter a loop to exercise signal lines to aid in debugging.

EPROM Checksum Test

The EPROM Checksum test verifies the EPROM has the correct program by adding up all the values in the EPROM. The test also verifies the 4 separate banks and the bank switching of the MC-12/MC-12 Balanced. First, the data in each of the 4 banks of the EPROM is added up. The checksum of each bank is reported to the Serial Debug Port. This performs an addition of the entire EPROM. The test verifies that the calculated checksum matches the checksum value stored in the EPROM. If an error occurs an attempt will be made to blink the STANDBY LED using a rate of a two blinks per several seconds, and the test will attempt to enter a loop to exercise signal lines to aid in debugging.

Z180 SRAM

The SRAM test will perform non-destructive testing on the SRAM.

The non-destructive test first saves the data in the location being tested. Then that location is tested by writing and reading patterns 0x00, 0xFF, 0x55, 0xAA, 0x01, 0x02, 0x04, 0x08, 0x10, 0x20, 0x40, and 0x80. The original data is then returned to the SRAM and the next location tested. Once each location in the SRAM is verified, a counting-memory check is done throughout the SRAM to test buss integrity. First, each byte in a special 32-byte section is written with a count. Then, starting from the beginning of the block, and incrementing through it, the count is verified to be correct. If so, this area will be used to store the contents of the rest of SRAM as it under goes the count check in 32-byte blocks. If an error occurs an attempt will be made to blink the STANDBY LED using a rate of a three blinks per several seconds, and the test will attempt to enter a loop to exercise signal lines to aid in debugging.

Flash Checksum Test

The Flash checksum test verifies the data in the flash memory. For all banks the checksum test adds up all the data in each bank except for the bank and stored checksum locations (stored in the last 3 locations of each bank.). The added value is then verified against stored values. If an error occurs an attempt will be made to blink the STANDBY LED using a rate of a four blinks per several seconds and the test will attempt to enter a loop to exercise signal lines to aid in debugging.

Display for the Remaining Tests

If the following tests fail, the VFD display and LED matrix will display the test and error fault, if one occurs, as previously discussed. The VFD will display the test number and the error code. In the event that the VFD is not operable, the same information will be written to the LED matrix. The test number will be read out as in the top row. The error number can be read out in the second row (Most Significant Byte) and third row (Least Significant Byte).

VFD Test

The VFD performs a busy test and a memory test. The busy test sends information to the VFD and verifies that the VFD asserts then de-asserts its busy status. The VFD memory test consists of writing 55h, and AAh, to the character generator memory and display memory space of the VFD and reading them back. After the MC-12/MC-12 Balanced has passed the VFD Test, for the rest of the power-on diagnostics, the VFD displays:

DIAGNOSTIC TESTS
…   …

The dots increment in number from both sides simultaneously, as the rest of the power-on diagnostic tests are completed. This keeps the user informed as to the functioning of a MC-12/MC-12 Balanced.

If a failure occurs, the test will attempt to write an entry into the error log and enter a loop to exercise signal lines to aid in debugging. The error log is stored in the non-volatile section of the SRAM so that it is not destroyed during the power-on diagnostics. A single error log entry is made each time the MC-12/MC-12 Balanced is powered up, a diagnostic test is executed, and a failure encountered.

IO FPGA

The I/O FPGA test loads and verifies the programming of the part. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

Digital Audio Receiver (DAR) FPGA

The DAR FPGA test loads and verifies the programming of the part. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

Audio FPGA

The Audio FPGA test loads and verifies the programming of the part. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

Analog FPGA

The Analog FPGA test loads and verifies the programming of the part. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

Crystal 43296 Boot Serial Protocol Interface

This test verifies that the Crystal 43296 can communicate with the Host processor. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

Crystal 8420 Boot Memory Test

This test verifies that the Crystal 8420 can communicate with the Host processor. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

SHARC SDRAM Test

This test verifies that the SDRAM for each SHARC that has this test enabled on the Main Board is operational and can be written to and read from. The SDRAM test is run on Pair 0 Processor A and on Pair 1 Processor C. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

The test writes the test patterns of 0x55555555, 0xAAAAAAAA, and 0x00000000 to each location and reads them back. Once each location is verified, a counting test is applied to verify the address buss.

SHARC SRAM Test

This test verifies that the SRAM for each SHARC that has this test enabled on the Main Board is operational and can be written to and read from. The SRAM tests is run on Pair 0 Processor B and on Pair 1 Processor D. If a failure occurs, the test will attempt to write an entry into the error log, write the test number and the error number to the VFD and LED matrix.

The test writes the test patterns of 0x55555555, 0xAAAAAAAA, and 0x00000000 to each location and reads them back. Once each location is verified, a counting test is applied to verify the address buss.

Power-on Diagnostics Completed

After the power-on diagnostics are completed the VFD will display the appropriate power up message:

MANUFACTURER MODEL VX.XX
(c) 2001 OPTIONS

At this point the operating system takes over the functioning of the MC-12/MC-12 Balanced.

EXTENDED DIAGNOSTICS TESTS

Entering Extended Diagnostic Tests

The extended diagnostic tests are accessible by pressing and holding the **RECORD LD** and **ZONE 2 LD** front panel buttons when powering on a MC-12/MC-12 Balanced. The audio outputs (analog and digital) are muted. After entering the diagnostics and the VFD displays LEXICON, the front panel buttons can be released. After the model banner is briefly displayed on the VFD, the display will indicate:

DIAGS MENU
FUNCTIONAL TESTS

The extended diagnostics can also be entered via the serial debug port by first entering the debug program. Typing ‘debug’ when connected to the serial port accesses the debug program (the debug program is case sensitive). In addition the extended diagnostics can be entered by sending ed, for extended diagnostics, to the unit via the serial debug port during the first 10 seconds after powering on the unit.

After extended diagnostics are entered, the front panel encoder, Mode Up and Mode Down buttons are used to navigate through the diagnostics. The front panel encoder is rotated to display the desired tests. The Mode Down button is pressed to move down through the menu selections and to execute the desired diagnostic test. The Mode Up is used to back up through menu selections similar to an escape button on a computer keyboard.

Types of Tests

The Extended diagnostic tests fall into two categories. The first category is for tests required to functionally verify an MC-12/MC-12 Balanced. These will be referred to as manufacturing diagnostic tests. The second category is for troubleshooting defective units. These tests are only utilized if there is a failure. The troubleshooting tests can be used to help isolate the source of failures. These tests are referred to as troubleshooting diagnostics.

Three groups of tests are executed for every MC-12/MC-12 Balanced. These are the Pre Burn-In Tests, Burn-In Loop, and the Manufacturing Suite. The Pre Burn-In, Burn-In, and Manufacturing suite comprise the automated sets of tests used to verify proper operation of the unit. Each of the tests in these suites are run in order unless there is a failure. The failing test will loop to allow the electrical signals to be active for troubleshooting. The user can optionally continue the suite. The Repair suite allows a technician to run particular tests for troubleshooting.

User Interface

The user interface consists of a set of menus. The top menu is the "DIAGS MENU" and is shown in the top line of the VFD display. To view the available menu items turn the encoder knob in either direction and the menu choices will appear in the second row. When the desired menu item is shown press the Mode Down button. This selects the menu item. If the item is another menu, the menu's title now appears in the top line of the VFD and its menu items are in the second row. If a test is selected, the test name will appear in the top line and the results or information to run the test will be on the second row. Once a test is finished, or to get out of a menu, press the Mode Up button.

The group tests are those diagnostics where if a test passes, the diagnostics automatically execute the next test. Group tests are the Power-On Diagnostics, the Manufacturing Suite, the Pre Burn-In test, and the Burn-In Loop. If one of the group tests is selected the next test is automatically run if the current test passes. Upon successful completion of the group tests the VFD will either display "Pass" or "Fail", come out of the test group to the menu or continuously loop as in the case of the Burn-In Loop test.

If a test fails, the VFD, and front panel LEDs, will attempt to indicate the failed test. The test will attempt to loop to keep the signal lines active for debugging purposes. If an individual test is selected, it will continuously run and report if it passes every time it successfully completes the test. If the test fails it will attempt to loop to keep the signal lines active for debugging purposes. In addition, test progress and failure information is available via the serial debug port. Specific failure information will depend on the test being executed. Pressing and holding the Mode Up button returns the user to the top level diagnostic menu.

EXTENDED DIAGNOSTICS SUITE

The Repair Diagnostic Suite allows one to run every diagnostic test on the unit. The Functional Suite uses the same tests as the Repair Diagnostic Suite, but automates how the tests are run.

The following tests are available in the Functional/Repair Diagnostics:

Extended Diagnostics Test List

Z180 EPROM checksum
Z180 FLASH checksum
Z180 SRAM
I/O FPGA Verify
RS232 Wrap Test
SHARC Tests
SHARC GPIO(x4)
- PAIR 0 PROC A
- PAIR 0 PROC B
- PAIR 1 PROC A
- PAIR 2 PROC B

SHARC SRAM (x4)
- PAIR 0 PROC A
- PAIR 0 PROC B
- PAIR 1 PROC A
- PAIR 2 PROC B

SHARC SDRAM (x4)
- PAIR 0 PROC A
- PAIR 0 PROC B
- PAIR 1 PROC A
- PAIR 2 PROC B

SHARC WCLK(x4)
- SEL 44 WORD CLK
- SEL 48 WORD CLK
- SEL 88 WORD CLK
- SEL 96 WORD CLK
- SEL 44-48 PLL WCLK
- SEL 88-96 PLL WCLK
- SEL DRCVR WCLK
- PAIR 0 PROC A
- PAIR 0 PROC B
- PAIR 1 PROC A
- PAIR 2 PROC B

SHARC Boot (x2)
PAIR 0
PAIR 1
DAR FPGA Verify
Audio FPGA Verify
CS49326 Boot Test
CS4820 ID Test
Analog FPGA Verify
IR Remote
VFD Memory Test
VFD CHAR Test
VFD BLOCK Test
OSD CHAR Test
SWITCH Test
LED Test
ENCODER Test
VIEW ERRORLOG
Clear NON-VOL SRAM
Set Triggers
Expand Output MUTE
Show Serial NUM
PIC SN Validity
Flash Burn Test
Normal Operation

The diagnostic tests that are the same as in the power-on tests are not described here.

RS232 Wrap Test

This test verifies the RS232 ports are working by comparing the transmitted signal (at pin 2 of J5) to the received signal (at pin 3s of J5). If the signals are the same, the test passed. In order to test this circuit, (2) RS232 Wraparound plugs are needed and must be installed at the female D9 connectors (J3 & 4) on the rear panel of the MC-12/MC-12 Balanced labeled “RS232”. Once these plugs are installed, the test can be executed.

When the test is selected, the display will read:

EXTENDED DIAGNOSTICS
RS232 Test

All buttons except for the Mode Down will be inactive. The ENCODER is active to select another test.

Pressing the Mode Down button will execute the test and the display will read the following if both ports pass:

SERIAL PORT A PASSED
SERIAL PORT B PASSED

If Serial Port A Failed, the display will read:

SERIAL PORT A Failed
SERIAL PORT B PASSED

If Serial Port B Failed, the display will read:

SERIAL PORT A PASSED
SERIAL PORT B Failed

If both Serial Ports Failed, the display will read:

SERIAL PORT A Failed
SERIAL PORT B Failed

To troubleshoot this type of failure, use the front panel Mode Down button. Each time the button is pressed, a message is sent out the RS232 port at pin2 of J4. Therefore, this will activate the COM0_TX0 signal coming from the Z180 pin 48. In the situation where the test passes, the COM0_RX signal is present at Z180 pin 49 as long as the wraparound plug is connected. Another way to test this circuit is to verify the IR Receiver (green) LED lights briefly when the button is pressed. This approach can be helpful when troubleshooting intermittent failures.

Note: If the unit is attached to a debugging PC, then serial port A will fail; however, if the PC's terminal software is showing results and the user is able to type in commands or run debug scripts, then the port is working.

IR Remote

This test verifies the functionality of the IR Remote by pressing on the remote and verifying that the VFD displays which IR remote button was pressed. The VFD displays in hexadecimal the code received when a remote key is pressed. The hex display on the VFD remains unchanged until another remote key is pressed. While the remote key is being pressed the IR acknowledge LED will flash and the VFD displays the message "IR", (without the quotes), next to the hex value. When you have successfully exited the test the VFD will display an arrow on the left side pointing to the word REMOTE.

When the test is selected, the display will read:

IR REMOTE
Remote Test:

All buttons except for Mode Down will be inactive.

When a button is hit (pressed/release) on the remote, the display will read;

IR REMOTE
Remote Test: 0C

When a button is held down on the remote, the display will read;

IR REMOTE
Remote Test: 0CIR

IR is displayed to indicate the remote is currently transmitting a signal.

VFD Character Test

The combination of the Character Test and the Block Test verifies that all display segments are functioning. The Character Test places the same character on all VFD segments. The ENCODER knob is then used to change the character. The test has sufficient variation of characters to verify complete functionality of the display. All characters present in the VFD can be observed.

When the test is selected, the display will read:

AAAAAAAAAAAAAAAAAAAA
AAAAAAAAAAAAAAAAAAAA

The operator will use the ENCODER knob to view other characters.

To exit the test, press the Mode Up button.

VFD Block Test

The Block Test illuminates all pixels on a single segment of the VFD. The ENCODER knob is then used to move the block to each segment.

Pressing the EFFECT DOWN button will execute the test and the display will read: ■

The operator will use the ENCODER knob to view the block and to move the block through all VFD locations. At the end of the line, the block will wrap to the next line. In the case of second line, the block will return to the starting point on the first line.

Switch Test

This test will verify all 43 front panel switches are working. Each button on the front panel is pressed and the VFD will indicate which front panel button has been pressed.

Example: Switch Test: MODE_DN in the second line on the VFD.

If the button has an LED associated with it, the LED will illuminate. When all switches have been tested the bottom half of the display will indicate completion.

LED Test

The LED test illuminates each LED by the tester turning the ENCODER knob clockwise or counter clockwise. As the ENCODER knob is turned each individual LED is illuminated.

Encoder

The Encoder Test verifies the operation of the Encoder including direction and the 24 positions. It is designed so if there was a bad position on the Encoder, the display will never indicate a "Passed" message. This is achieved by having the accumulator value reset to 0 if a switch position is bad or if the Encoder was turned in the opposite direction during the test. Therefore, the accumulator never sees the expected value of 24, so the program isn't able to perform the next task (i.e. instruct the user to perform the counter-clockwise test or display "Passed").

When the Encoder is being tested, the bottom right half of the display will indicate the Encoder direction and position value. The test requires the clockwise direction to be tested first.

When the ENCODER is being turned clockwise the display will read:

EXTENDED DIAGNOSTICS
Encoder Test CW 05

In this example, the Encoder was turned 5 positions clockwise.

After the ENCODER is turned 1 revolution clockwise, covering all 24 positions, the display will read:

EXTENDED DIAGNOSTICS
Encoder Test CCW 24

The bottom half of the display (CCW 24) indicates the counter-clockwise test is ready to be executed.

After the ENCODER is turned 1 revolution counter-clockwise, covering all positions, the display will then read:

ENCODER TEST
Encoder test passed

View Error Log

This is not a test but it enables an operator to view the contents of the error log. Turning the encoder allows the operator to view the log contents.

Clear Non-Volatile RAM

This is not a test, but allows the operator to clear out the error log contents and other areas of RAM that are not cleared on a power up.

When the user selects this menu item the display will show:

CLEAR NON-VOL SRAM
Confirm - Press MUTE

When the **MUTE** key is pressed, the second line will display:
Initializing RAM

then it will display:
Test: Pass

Functional Suite

The Functional Suite is available from the top level DIAGS MENU when the FUNCTIONAL TESTS item is selected.

When the operator selects that menu item, the VFD will display:

FUNCTIONAL TESTS
START ALL TESTS

There is only one menu item in this menu, and selecting it will start the sweep through the whole repair suite. As long as there are no errors, the test will continue until the tests requiring an operator response are encountered. If there is a failure, the offending test will cycle and the error code will be displayed on the 2^{nd} line. For example, if the analog FPGA verify fails the VFD will show:

ANLG FPGA TEST
Fail E:0A.

If the operator wants to continue, he can hit the Mode Up button.

Some tests require the operator to help with the test. This may be just to hit the Mode Up button or it may require the operator to turn the encoder to iterate through the test.

Upon completion of all of the tests, the 2^{nd} row of the VFD shows Pass or Errors.

LOOP Tests

Entering LOOP Tests

The Loop (burn-in) suite is available from the top level DIAGS MENU when the LOOP TESTS item is selected.

When the operator selects that menu item, the VFD will display:
LOOP TESTS
NON_VOL RAM SETUP

The NON_VOL RAM setup initializes the non-volatile section of the SRAM with a byte that is verified by the loop tests. As the unit is in burn-in, this byte is continuously verified ensuring that the register section of the SRAM continues to hold data.

Rotating the encoder knob will display the following on the VFD:

START ALL TESTS

When the Start All Tests menu option is selected the Loop tests are run continuously. These are the tests available in the Loop Test Suite:

List of LOOP Tests

Z180 EPROM checksum
Z180 FLASH checksum
Z180 Burn-In SRAM
I/O FPGA Verify ID
SHARC Internal GPIO(x4)
SHARC SRAM (x4)
SHARC SDRAM (x4)
SHARC Boot (x2)
DAR FPGA Verify ID
Audio FPGA Verify ID
Analog FPGA Verify ID
Crystal 49326 Boot
Crystal 4820 Verify ID

There is only one menu item in this menu and selecting it will start the sweep through the whole suite of loop tests. As long as there are no errors the test will continue to run. If there is a failure, the entire bottom row of 9 LEDs on the front panel will light. These are the TAPE, TUNER, and AUX LEDs for the Main, Zone 2, and Record sections. Depending upon the failure, the failing test will cycle and the error code will be displayed on the second line of the VFD. For example, if the analog FPGA verify fails the VFD will show:

ANLG FPGA TEST
Fail E:0A.

If the user wants to continue, press the Mode Up switch.

Upon completion of all of the tests, the second row of the VFD will briefly indicate Pass or Errors.

Loop SRAM test

The Burn-In SRAM Test reads a bit-pattern from a known location by the NON_VOL RAM SETUP Test.

Audio I/O Tests

The Audio I/O tests contain the following tests:

Audio Input 1 Test
Audio Input 2 Test
Audio Input 3 Test
Audio Input 4 Test
Audio Input 5 Test
Audio Input 6 Test
Audio Input 7 Test
Audio Input 8 Test
S/PDIF Input CX1 Test
S/PDIF Input CX2 Test

S/PDIF Input CX3 Test
S/PDIF Input CX4 Test
S/PDIF Input CX5 Test
S/PDIF Input CX6 Test
S/PDIF Input OP1 Test
S/PDIF Input OP2 Test
S/PDIF Input OP3 Test
S/PDIF Input OP4 Test
S/PDIF Input OP5 Test
S/PDIF Input OP6 Test
AES/EBU Input Test

These tests put the unit into a state to pass audio through the path that is contained in the test name for troubleshooting. For instance the Audio Input 1 Test will pass analog audio from analog input 1 to all the outputs.

Video I/O Tests

The Video I/O tests contain the following tests:

INIT INT SYNC
INIT EXT SYNC
Select PAL
Select SECAM
Load Font
Color Bars
Show CHARS

The video I/O tests initialize the video circuitry to put the unit into a known state for troubleshooting. The menu items select a few of the basic setups that can be used for troubleshooting. These selections will instruct the On Screen Display (OSD) IC in the unit to output a video signal that can be used to verify the video circuit from the OSD to the monitor outputs of the unit.

Service Notes

This section will address some of the descriptions and issues that involve the unit in order to repair and/or replace boards or components in the MC-12/MC-12 Balanced. Please refer to the Assembly Drawings found in Chapter 8 and additional drawings/figures that have been included in this section.

CAUTION

Please refer to the Safety Suggestions and Summary Descriptions at the beginning of this manual.

REMOVING THE TOP COVER

1. Remove the 12 screws that hold the top cover of the unit as shown in Figure 1 below.
2. Reverse the above procedure when reinstalling the cover.

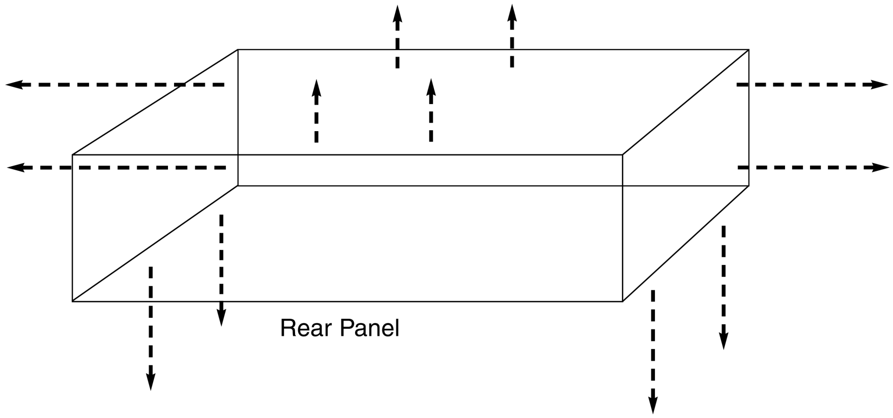


Figure 1

REMOVING THE VIDEO AND ANALOG BOARDS

1. First rotate the MC-12/MC-12 Balanced so the rear panel is facing you.
2. Disconnect the following cables using Figure 2 as a guide.
   2.A. The ribbon cable connecting the Main Board to the Video Board. Disconnect the cable from its location J26 on the Main Board by gently rocking the cable from side to side and pulling it away from the board.
   2.B. The ribbon cable connecting the opto/mic board to the analog board. Disconnect the cable from its location J30 on the analog board. (The opto/mic board is located between the Main Board and the analog board, directly behind the Microphone Inputs on the rear of the panel.)
   2.C. The ribbon cable connecting the analog board to the Main Board. Disconnect the cable from its location J29 on the Main Board by releasing the locking tabs on the sides of the connector then pulling the cable away from the board.
   2.D. The power supply cable from its location J26 on the analog board. The power supply cable may require more force to remove than the other cables.
   2.E. The power cable connecting the analog board to the Video Board. Disconnect the cable from its location J25 on the analog board.

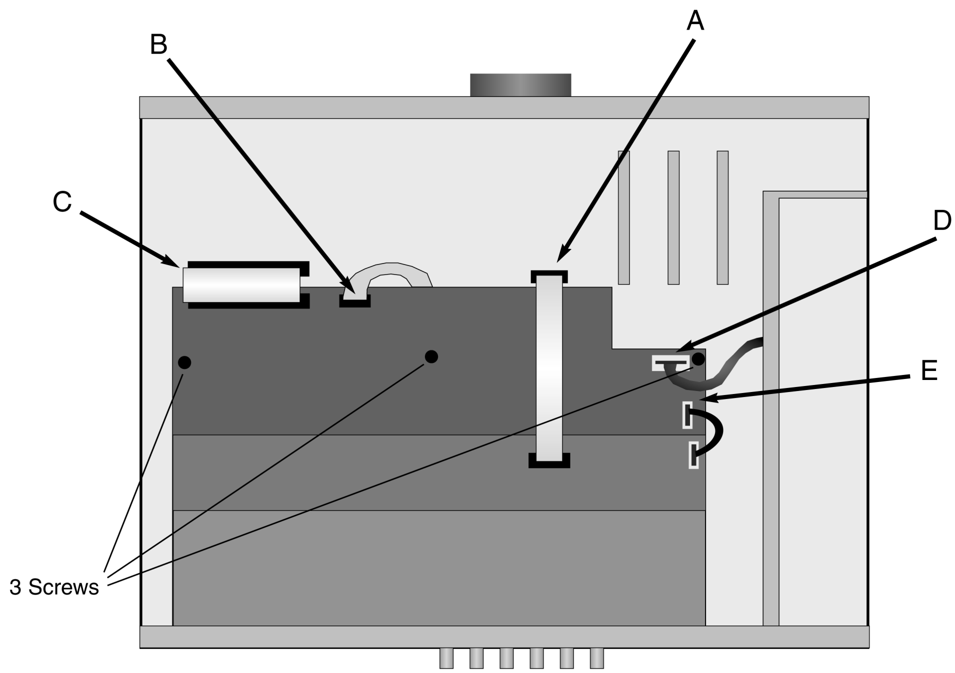


Figure 2

3. Refer to 080-14530 ASSY DWG,CHASSIS in chapter 8 and remove the five rear panel screws that are connected to the Video Board.
4. Carefully pull the board inward then up and out of the MC-12/MC-12 Balanced. Store it in a static-free area.
5. Next remove the five rear panel screws that are connected to the analog board.
6. Next, remove the three internal screws connecting the analog board to the chassis. These screws are black. DO NOT REMOVE THE SILVER SCREWS.
7. As done with the Video Board carefully pull the analog board inward then up and out of the MC-12/MC-12 Balanced. Store it in a static-free area.

REMOVING THE MEMORY BOARD

1. With the MC-12/MC-12 Balanced front panel facing you locate the memory board mounted to the inside chassis on the Right front side of the MC-12/MC-12 Balanced.
2. Remove the screw at the top of the board that holds it to the chassis.
3. Carefully pull the board up and out of its connector J39. Store it in a static-free area.

REMOVING THE POWER SUPPLY BOARD

1. With the MC-12/MC-12 Balanced front panel facing you, locate the power supply module mounted to the inside chassis on the left hand side of the MC-12/MC-12 Balanced.
2. At the back left corner, locate the wires that are attached to the rear power switch and remove them from the switch.
3. Hold the supply with one hand and remove the 2 nut screws that hold the supply to the inside chassis.
4. Rotate the far end of the supply up out of the chassis and then disconnect the 2 secondary wire connections from the other side of the power supply.
5. Store it in a static-free area.

REMOVING THE FRONT PANEL

1. Just behind the front panel you will need to locate 2 ribbon cables J35 and J33. Carefully remove them from the connectors on the Main Board.
2. Remove the 2 screws from the inside top left and right corners of the front panel.
3. At this time tip the MC-12/MC-12 Balanced carefully on its side and locate and remove the 3 remaining screws on the bottom that hold the front panel.
4. Remove the front panel and store it in a static-free area.

CHANGING TRIGGER VOLTAGE FROM 12 VOLTS TO 5 VOLTS

1. With the Video and Analog boards removed as described above and the MC-12/MC-12 Balanced front panel facing you, locate the 6 jumpers to the trigger circuit in the upper rear left hand corner of the Main board.
2. All the jumpers W 1-6 are jumpered on pins 1 and 2 for 12 volt trigger output. To make them all 5 volt trigger out, all the jumpers must be moved to pins 2 and 3.

REMOVING THE MAIN BOARD

Removal of the Main Board can only be done after removal of the Video and Analog boards.

1. Locate and remove the 7 screws and 3 standoffs holding the Main Board to the chassis.
2. Using the same diagram locate and remove the 8 screws, 5 dress nuts, 4 nut screws, and the trigger connector.
3. Carefully remove the Main Board from the chassis and store it in a static-free area.

INITIALIZATION (HARD RESET) PROCEDURE

This is the initialization procedure for the MC-12/MC-12 Balanced.

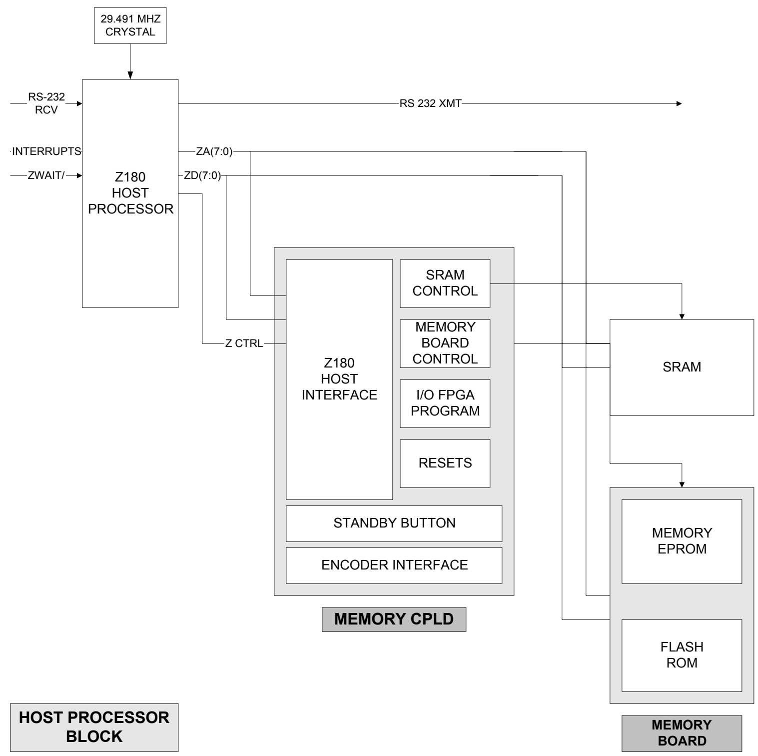
CAUTION This procedure will clear all custom settings in the MC-12/MC-12 Balanced.

1. Power down the MC-12/MC-12 Balanced main power switch on the back of the MC-12/MC-12 Balanced.
2. Press and hold down 2 buttons on the front panel: the Zone 2 LD button and the Record LD button.
3. While holding down those buttons turn on the Main power switch on the back of the unit.
4. Once the unit shows activity on the front panel, release the buttons.
5. When the front panel reads DIAGS MENU FUNCTIONAL TESTS turn the volume knob on the front panel so that it reads DIAGNOSTICS MENU REPAIR TESTS.
6. Press the Down Mode button once. The display reads REPAIR TESTS Z180 EPROM CHECKSUM.
7. Turn the Volume knob until the display reads REPAIR TESTS CLEAR NON-VOL SRAM.
8. Press the Down Mode button once. The display reads REPAIR TESTS Confirm - Press MUTE.
9. Press the Mute button on the front panel once. The display will quickly read REPAIR TESTS Initializing RAM then read REPAIR TESTS Test completed.
10. Press the Up Mode button once. The display will read REPAIR TESTS CLEAR NON-VOL SRAM.
11. Turn the Volume knob until the display reads REPAIR TESTS NORMAL OPERATION.
12. Press the Down Mode button once. The display will flash DIAG Menu Please Wait. It will then go through a normal power up diagnostic test and drop into normal operation

Chapter 6 Theory of Operation

Main Board

Z180 HOST PROCESSOR



Z180 (schematic page1)

The Z180 is responsible for all systems control in the unit. It runs off the 29.491MHz crystal oscillator. It is reset by the main **PWR_RST/** signal. ZCLK is a buffered synchronous clock output that is used to synchronize signals in the Memory CPLD and the I/O FPGA. One half of a VHCT244 is used to buffer **ZA(3:0)** to the DAR FPGA because of the length of signal trace.

Memory CPLD (schematic page1)

The Memory CPLD is programmed at the factory like an EPROM. It can be programmed before or after it is soldered to the PC board. It provides the following functionality:

- Host data, address and control interface – provides all memory space address decoding, plus a small section of I/O space that is occupied by the Memory CPLD internal control and status registers
- SRAM read/write signals and bank address bit
- Flash ROM and EPROM control signals and bank address bits, **RA(22:15)**
- The I/O FPGA programming bits
- Reset lines under host control to the Video Board, Analog Board, I/O FPGA and Front Panel Board
- The Standby LED
- The Standby Button
- The Front Panel Encoder interface

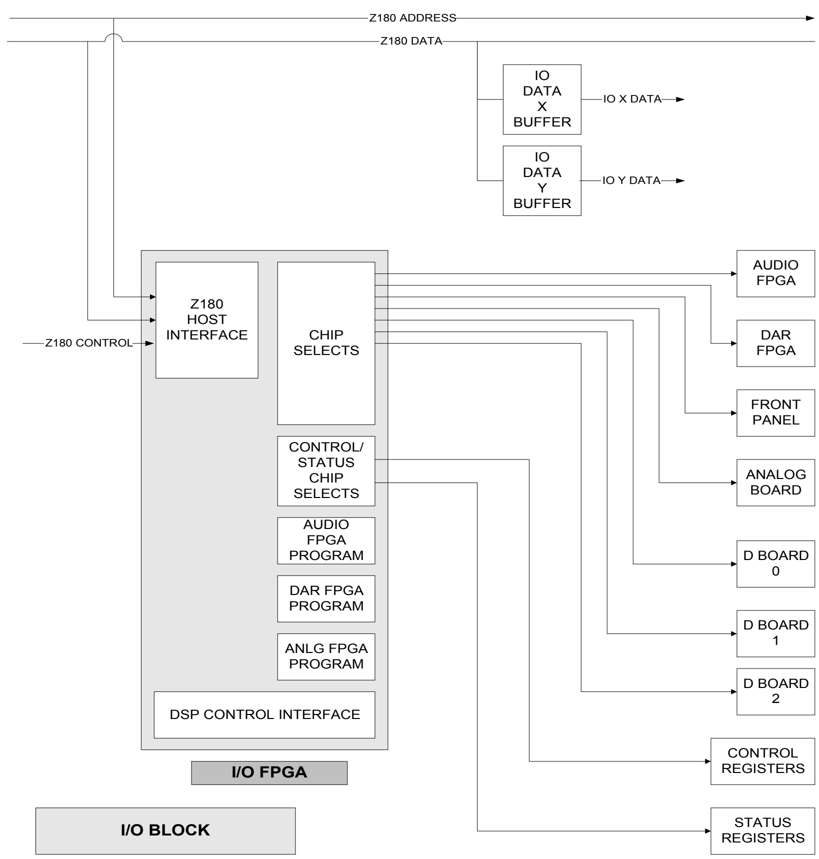
Host Processor Memory (schematic page 2 and Memory Board)

There are three devices located in the Z180's memory space; the SRAM, which is on the Main Board, and the FLASH ROM and EPROM, which are located on the Memory Board. The 32kx8, 70ns SRAM is powered by the battery backup, **BAT_VCC**, so that user and factory default settings are preserved when the unit is powered down.

The Z180 boots from the 256kx8 70ns EPROM at power up. Once the EPROM, SRAM and FLASH diagnostics have passed, the Z180 sets a bit in the Memory CPLD that allows the Z180 to run out of the FLASH ROM. The 2Mx8 FLASH ROM is programmable from the RS-232 serial port.

Host Processor I/O (schematic page 2 and 3)

All peripheral devices and boards live in the Z180 I/O address space. All address decoding is handled by the I/O FPGA. Because of the size of the Main Board, the Z180 data bus is buffered through two 74VHCT245s, creating the **IODX** and **IODY** data buses. All data and address buses going to other boards are also buffered.



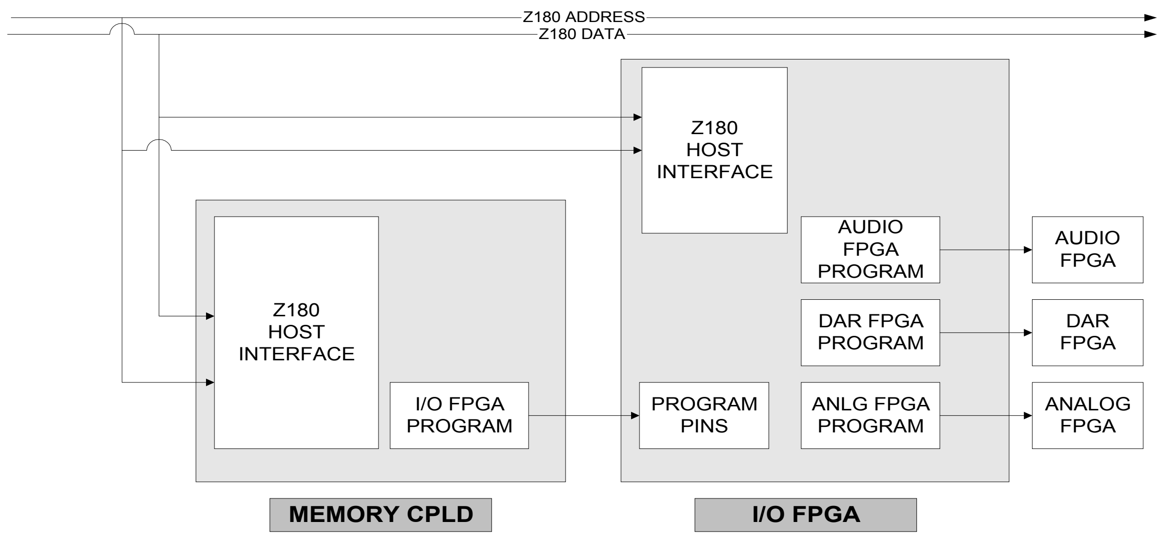
RS-232 Serial Interface (schematic pages 1 and 20)

The 29.491MHz crystal oscillator is divided down to provide the 19.2K Serial Baud Rate of the MC-12. The TX0, RX0, TX1 and RX1 ports on the Z180 are connected to theMax202E Transceiver that drives the two female DE9 connectors RS-232 1 and 2.

FPGAS

Host Programming of FPGAs (schematic pages 1 and 2)

The FPGAs are programmed by the Host processor as part of the boot process when the unit is powered on from the rear panel. The I/O FPGA is programmed by the host through the Memory CPLD. The two remaining FPGAs, I/O and Audio, are programmed by the host through the I/O FPGA. It is important to understand that until the FPGAs have been programmed, most of the unit, including the front panel and on screen display, are in reset. There are LEDs that light to indicate when the programming for each FPGA is complete.

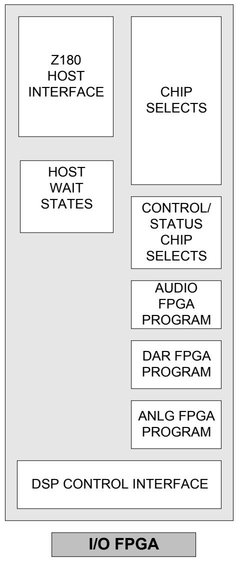


FPGA PROGRAMMING

I/O FPGA (schematic page 2)

The I/O FPGA has only a four-bit wide data path for the host interface. It provides the following functions:

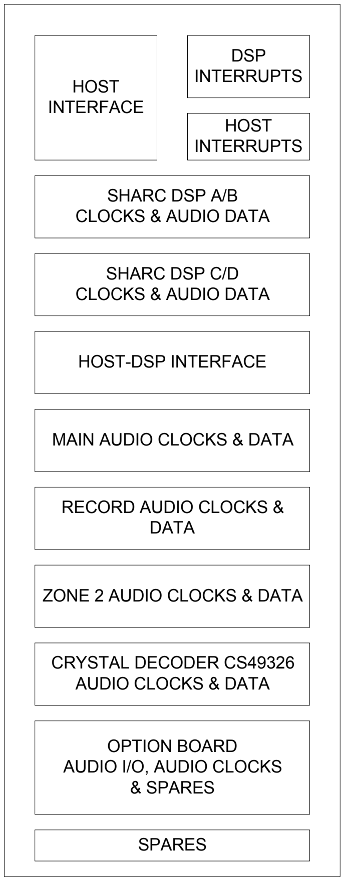
- Handles the entire I/O space memory map for the system.
- Generates the chip selects for all peripheral devices that the host communicates with over the I/O data bus.
- Automatically generates wait states to the Host for devices that require longer access times.
- Outputs the bits that are used to program the other FPGAs in the system.
- Provides the host side of the Host-DSP communication interface.



Audio FPGA (schematic page 4)

The Audio FPGA is the central audio routing block for the system. It performs the following functions:

- Generates word and bit clocks for each zone from the master clocks and distributes them to all audio devices and interfaces on the Main Board.
- Routes all I^2S audio data in the system.
- Packs and unpacks I^2S audio into octal streams for the SHARC DSPs.
- Provides interrupts to the SHARC and Crystal DSPs and the Z180 Host processor.
- Provides the DSP side of the Host-DSP communication interface.

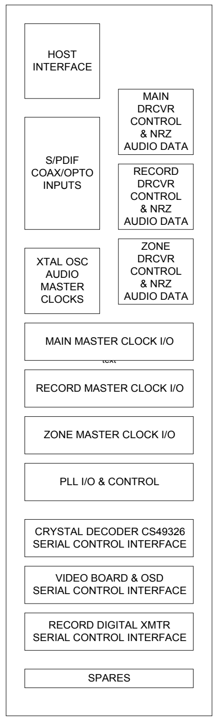


AUDIO FPGA BLOCK

DAR FPGA *(schematic page 16)*

This FPGA provides the following functionality:

- Allows the host to select which digital audio connector is connected to the Main, Record and Zone 2 Digital Receivers.
- Allows the host to choose between the crystal oscillators for analog audio, the master clock output of the Digital Receivers or the output of the Phase Lock Loop as the master clock source for each zone.
- Digital control signals for the Phase Lock Loop
- Control bits and sample-rate detection clocks to the Main, Record and Zone 2 Digital Receivers.
- Host Serial Control Interface to the Crystal 49326 DSP Audio Decoder. Consists of the chip select, serial clock and data. The FPGA converts the host parallel data to a serial data stream. It also converts the serial output of the Crystal chip to parallel for the host to read.
- Host Serial Control Interface to the Video Board and On Screen Display. Consists of the chip select, serial clock and data. The FPGA converts the host parallel data to a serial data stream.
- Host Serial Control Interface to the Record Digital Transmitter. Consists of the chip select, serial clock and data. The FPGA converts the host parallel data to a serial data stream. It also converts the serial output of the Crystal chip to parallel for the host to read.
- The 1MHz clock signal used by the 16C54 PIC IR Receiver.



DAR FPGA BLOCK

HOST INTERFACE TO OTHER BOARDS

Switch/LED, IR/Encoder, and VFD (schematic page 21)

The interface to the all of the front panel boards (with the exception of the standby board) is a single ribbon connector. All signals are connected to the Switch/LED Board. It then passes signals as required to the IR/Encoder Board and the VF Display.

The Signals used by the Switch/LED Board are as follows:

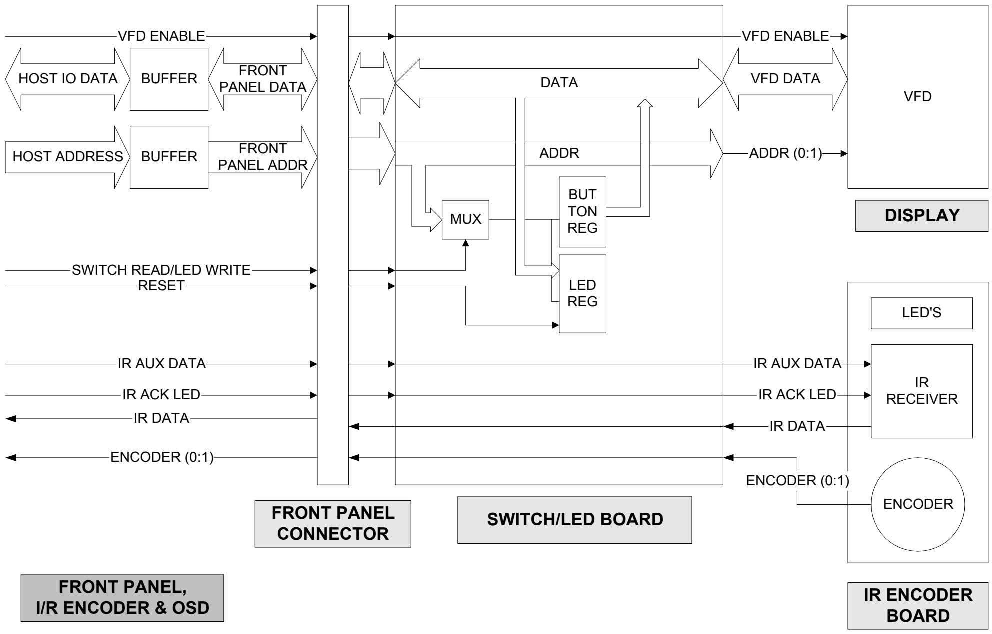
- FP_RST – This prevents the LEDs from lighting when the unit is first powered up, until the host is initialized.
- SWRD_LEDWR/ - When this signal is high, the MUX generates the enable for reading the Switch Buffer. When it is low, it generates write strobes to the LED Registers and the Switch Column register. In order to read the switches; the host must first select a column.
- Front Panel data – bi-directional
- Front Panel address – used by the MUX

Signals used by the VF Display are as follows:

- VFD_EN_BUF – chip select to the display
- Data – byte-wide
- Address – two address bits. Address determines whether an access is a read or a write.

Signals used by the IR/Encoder Board are as follows:

- IR auxiliary data from the rear panel connector. This is optically coupled with the incoming IR signal at the IR receiver.
- The IR acknowledge LED bit. This comes from the PIC and is used to indicate that the unit is detecting an infrared signal.
- System_On and Overload LED bits.
- Encoder 0:1 – these are the output of the Front Panel Encoder knob. They are read and interpreted on the Main Board.

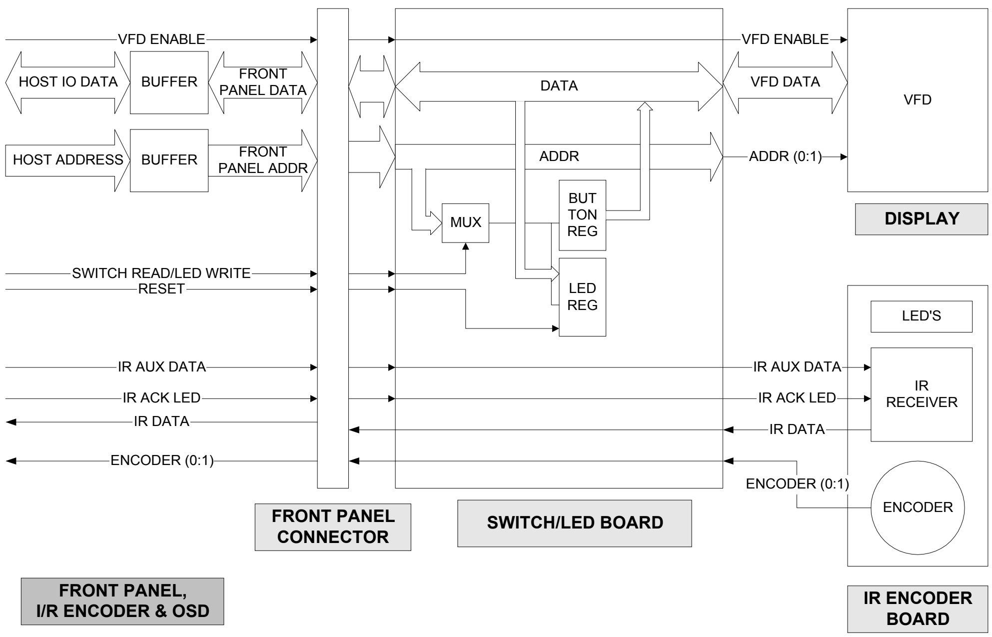

VFD ENABLE
HOST IO DATA
BUFFER
FRONT PANEL DATA
HOST ADDRESS
BUFFER
FRONT PANEL ADDR
SWITCH READ/LED WRITE
RESET
IR AUX DATA
IR ACK LED
IR DATA
ENCODER (0:1)
DATA
ADDR
MUX
BUT TON REG
LED REG
VFD ENABLE
VFD DATA
ADDR (0:1)
VFD
DISPLAY
LED'S
IR AUX DATA
IR ACK LED
IR DATA
IR RECEIVER
ENCODER (0:1)
ENCODER
FRONT PANEL CONNECTOR
SWITCH/LED BOARD
FRONT PANEL, I/R ENCODER & OSD
IR ENCODER BOARD

VIDEO BOARD & OSD

(schematic page 21)

The control interface to the Video Board consists of:

- Serial control data
- The serial control bit clock
- OSD chip select – enables the serial control port of the On Screen Display chip
- Video Register chip select – enables the serial to parallel registers that generate the control bits used on the Video Board.
- The video reset line

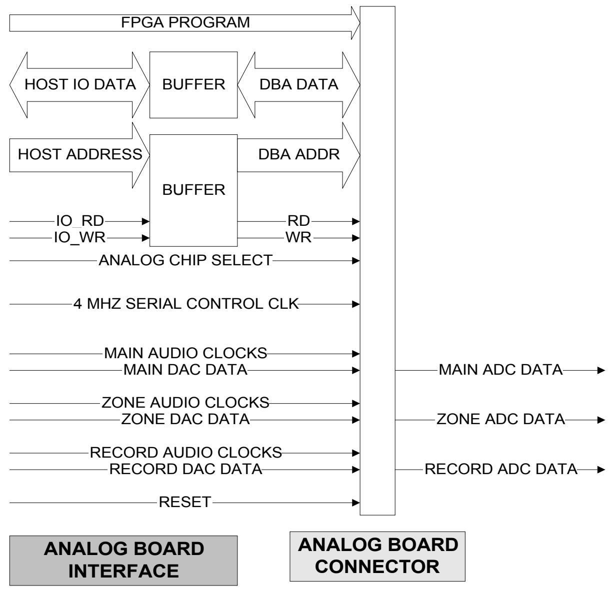


ANALOG BOARD

(schematic page 12)

The analog board has the following interface:

- FPGA programming bits
- Host I/O data bus
- Host I/O address bus
- Host I/O control – RD, WR and CS
- Reset
- 4 MHz clock used on the analog board to derive serial control clocks
- Main audio clocks and data
- Record audio clocks and data
- Zone 2 audio clocks and data

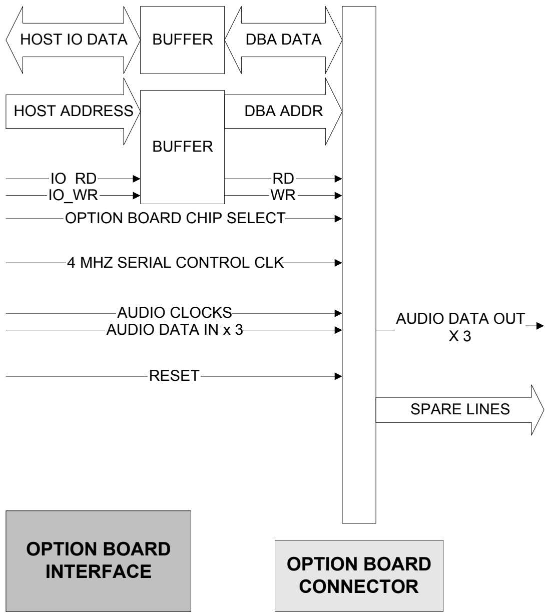


OPTION BOARDS

(schematic pages 13-15)

The option board connectors have the following interface:

- Host I/O data bus
- Host I/O address bus
- Host I/O control – RD, WR and CS
- Reset
- 4 MHz clock used on the analog board to derive serial control clocks
- Main audio clocks
- 3 audio input lines, may be 2- channel or octal
- 3 audio output lines, may be 2- channel or octal
- spare lines to/from FPGAs



DSP

Crystal 49326 DSP Audio Decoder (schematic page 5)

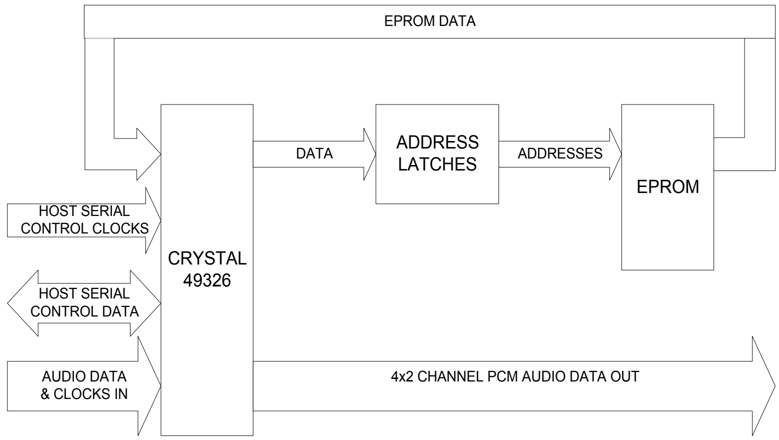
The Crystal DSP is responsible for detecting and decoding all compressed audio data formats, Dolby Digital and DTS. It is a 2.5-Volt part. Its master clock, DEC_24MHZ, is derived from the audio crystal oscillator.

To boot the chip, the Host processor sets the **DEC_ABOOT/IRQ** pin low and sets the **DECODER_RST/** pin high. The chip then boots from the external EPROM. During run time, the host communicates with the Crystal Decoder through a serial control interface that consists of:

- DECODER_DATA_IN – host serial control data generated in the DAR FPGA
- DECODER_DATA_OUT – Crystal Decoder status data output to the host.
- DECODER_SCLK – serial data bit clock
- DECODER/ - serial port chip select
- DEC_ABOOT/IRQ/ - Crystal Decoder interrupt to the host

The Main zone input, analog or digital is always routed through the Crystal decoder. The serial audio interface consists of:

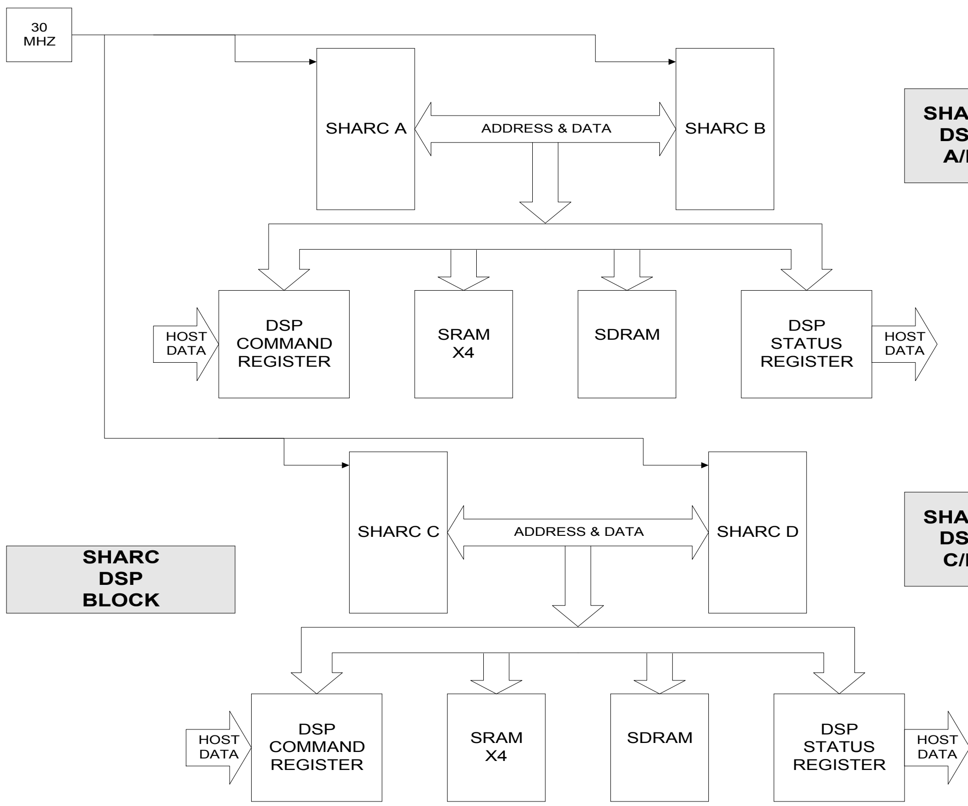
- DECODER_SDI – 2 channel PCM audio stream from either the Main Digital Receiver or the Main Analog ADC
- DECODER_SDO(3:0) – four 2-channel PCM audio streams going to the Audio FPGA
- DECODER_FSI – word clock audio framing signal, 1 x sample rate
- DECODER_SCKI **–** audio bit clock, 64 x sample rate



CRYSTAL DSP BLOCK

SHARC DSPs (schematic pages 6 – 11)

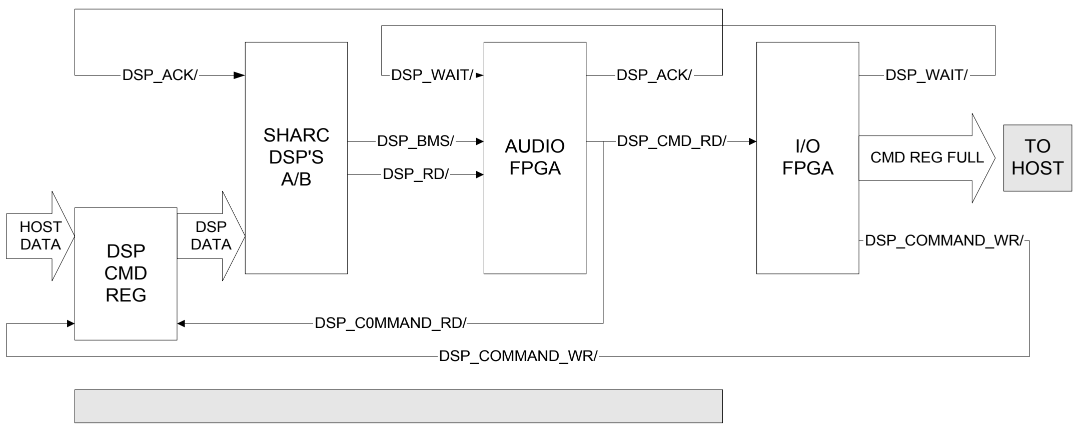
The principle DSP in the system consists of two pairs of Analog Devices 21065 SHARC DSP engines. Each pair shares four 128kx8 12ns SRAMs and one 2Mx32 SDRAM. The SHARCs communicate with this external memory and each other over a 32-bit wide data bus. All necessary chip selects are generated by the SHARCs, including the clocking required for the Synchronous DRAM. The SHARCs master clock is provided by a 30 MHz crystal oscillator that is distributed through a 74LCX14 inverter used as a buffer.



Host Communication with the SHARC DSPs *(schematic pages 2,4,6 –11)*

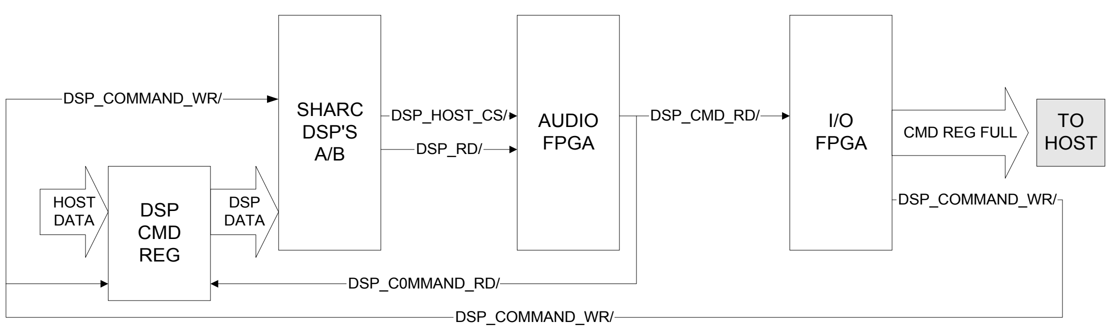
The lowest byte of the external data bus is also connected to the Host-to-DSP Command Register, a VHC574, and the DSP-to-Host Status Register, an HCT574. There are three modes of communication between the Host and the DSPs.

The first occurs at boot time. When it comes out of reset the A or C SHARC asserts **DSP_BMS/** and **DSP_RD/.** These are combined by the Audio FPGA to create **DSP_CMD_RD/.** This signal goes to the I/O FPGA where it is used to generate the **DSP_WAIT/** signal. DSP_WAIT/ is then returned to the Audio FPGA where it is re-clocked by the **DSP_30MHZ** to synchronize it to the SHARCs. It is then sent to the SHARC as **DSP_AB_ACK** where it keeps the SHARC in a wait state until the Z180 has written the data to the Host-to-DSP Command Register.



Host Writes Data to a SHARC DSP *(schematic pages 2,4,6 –11)*

This is how the host transmits data to the SHARCS during run-time. The Host writes a byte to the Host-to-DSP Command Register. The write strobe, **DSP_COMMAND_WR/** also interrupts the SHARC to let it know that a byte is waiting. The SHARC then retrieves the byte by asserting **DSP_HOST_CS/** and **DSP_RD/.** This also clears a status bit in the I/O FPGA letting the host know that the command register is empty and can be written to again.

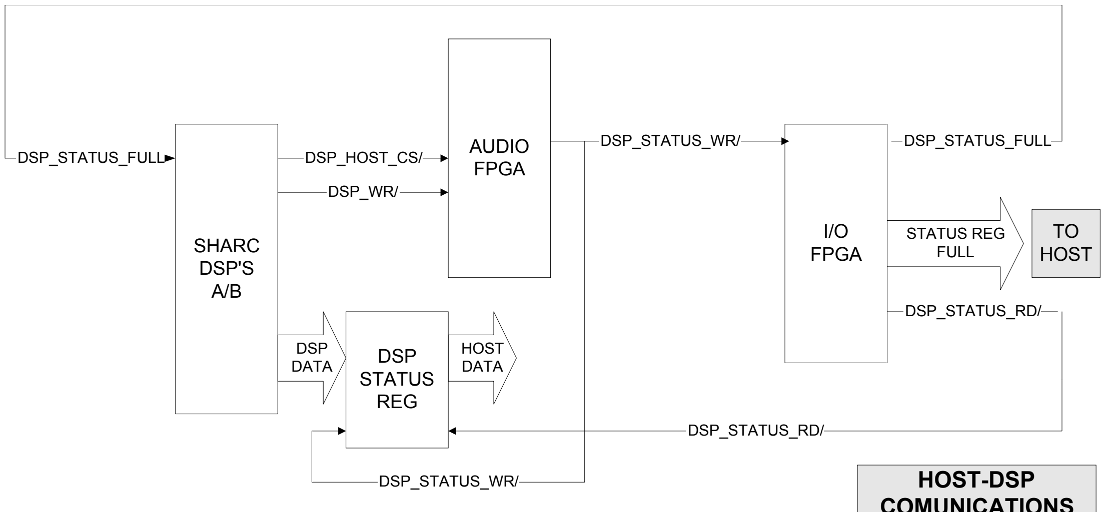


HOST WRITES DATA TO SHARC

SHARC DSP writes Data to the Host *(schematic pages 2,4,6 –11)*

The SHARC writes a byte into the DSP to Host Status Register by asserting **DSP_HOST_CS/** and **DSP_WR/.** This sets a bit in the I/O FPGA that lets the host know that that register is full and waiting to be

read. When the host reads the byte, the DSP_STATUS_FULL line to the SHARC is cleared so the SHARC knows that the register is empty and can be written to again.

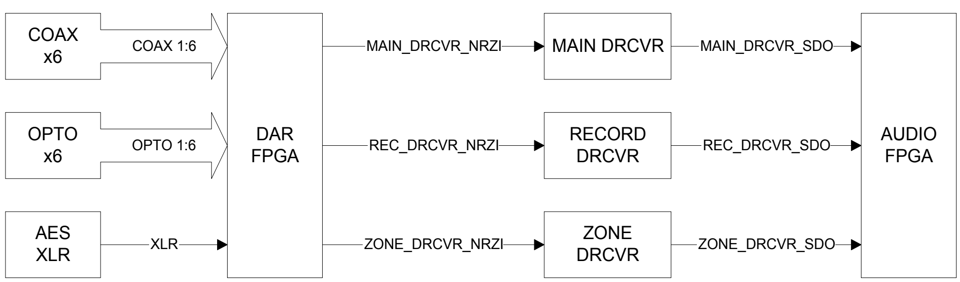


SHARC DSP WRITES DATA TO HOST

AUDIO ROUTING

Digital Audio Input Path (schematic pages 4, 16 and17)

Digital Audio can be either PCM 2-channel data or one of the compressed data formats. It enters the unit on one of the digital input connectors that are connected to the DAR FPGA. The FPGA functions as a mux and routes the output NRZ (Non Return to Zero) data of the connector selected by the user to the three Digital Receivers, Main, Record and Zone. These receivers lock to the incoming signal and extract a 2-channel PCM audio signal that is sent to the Audio FPGA.

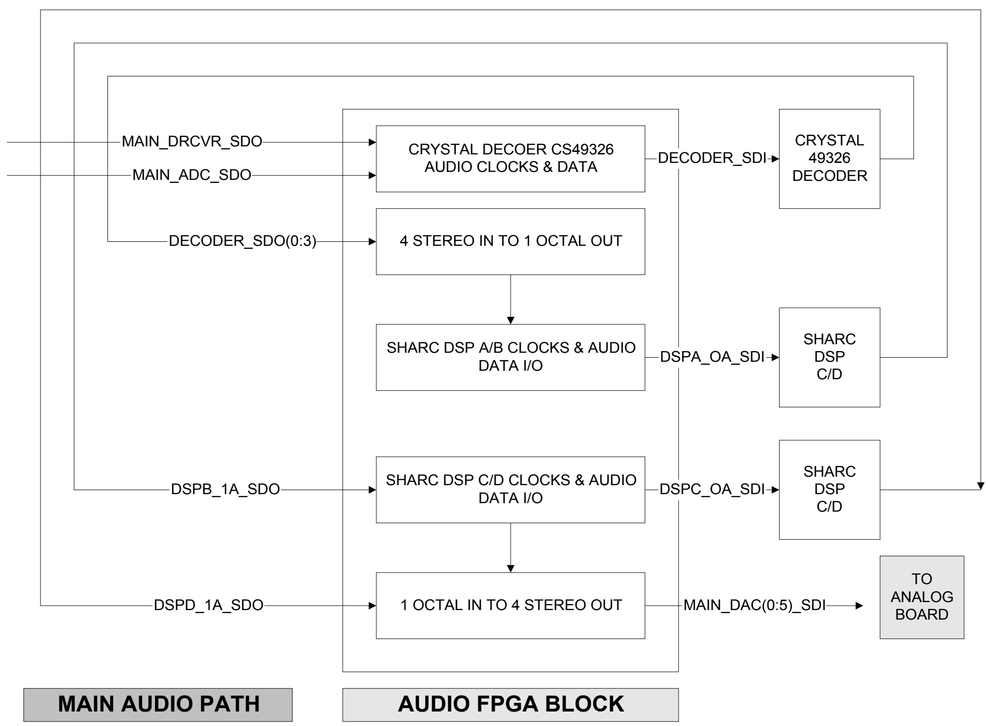


DIGITAL AUDIO INPUT PATH

Main Audio Data Path   (schematic pages 4, 5, 6 – 11, and 17)

The Main Audio Data Path is as follows:

1. Output of the Main Digital Receiver and the Main ADC to the Audio FPGA
2. Output of the Audio FPGA to the Crystal 49326 Decoder
3. 4 2-channel outputs from the Crystal 49326 Decoder back to the Audio FPGA
4. The 4 2-channel streams are packed into a single octal data stream in the Audio FPGA
5. The output of the octal packer is sent to SHARC A
6. The octal output of SHARC B is sent back to the Audio FPGA
7. The octal output of the Audio FPGA is sent to SHARC C
8. Two octal outputs of SHARC D are sent back to the Audio FPGA
9. The two octal outputs of SHARC D (not all slots are used) are unpacked into 6 2-channel PCM streams in the Audio FPGA
10. These 6 2-channel streams are sent to the Analog board as **MAIN_DAC(0:5)_SDI**



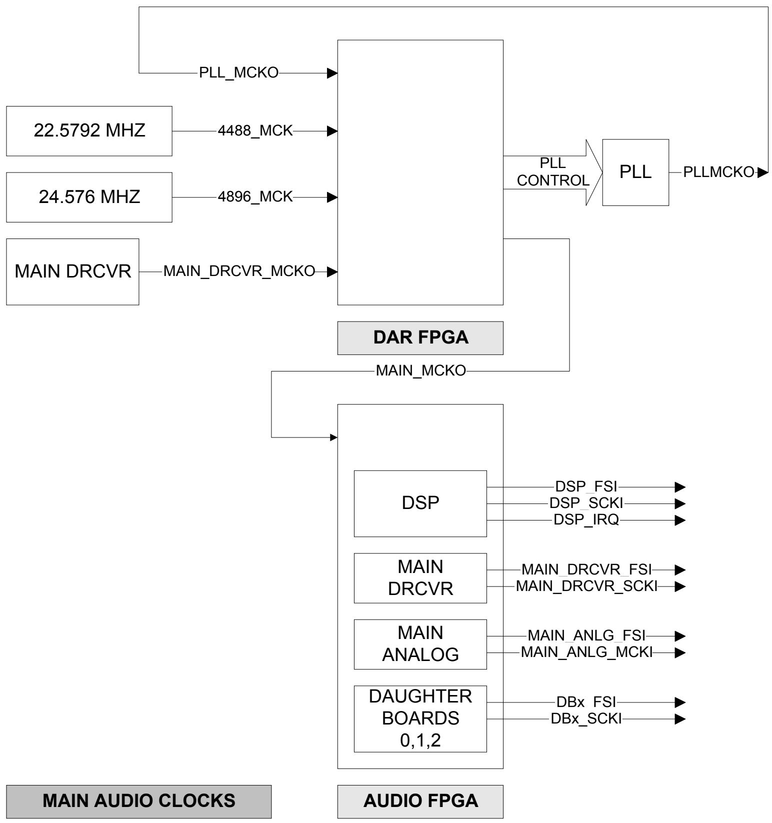
Main Audio Clock Path (schematic pages 4, 16, 17 and 18)

There are three possible sources of master clock for the Main Audio Path. The 22.5792MHz crystal oscillator that provides either a 44.1kHz or 88.2kHz sample rate, the 24.576 oscillator that provides either a 48kHz or 96kHz sample rate, or the master clock output of the main digital receiver. In practice, the unit runs off the crystal at 96kHz when the input is analog. When the input is digital, the master clock output of the digital receiver is used. This master clock is de-jittered by the Phase Lock Loop that is controlled by the DAR FPGA using signals derived from **MAIN_DRCVR_MCKO**.

Depending on the input selected, the appropriate master clock is routed from the DAR FPGA to the Audio FPGA. Here it drives a clock tree that divides down the master clock, which is 256 times the sample rate, 256FS, to create the other clock rates required.

- The SHARC DSPs receive a word clock, or framing signal, FS and a bit clock of 256FS
- The Digital Receiver uses a word clock, FS, and bit clock, 64FS

- The Analog Board and Option Boards receive a 256FS Master Clock and a word clock, FS. These are used on each individual board to derive the audio clock signals required by that particular board.

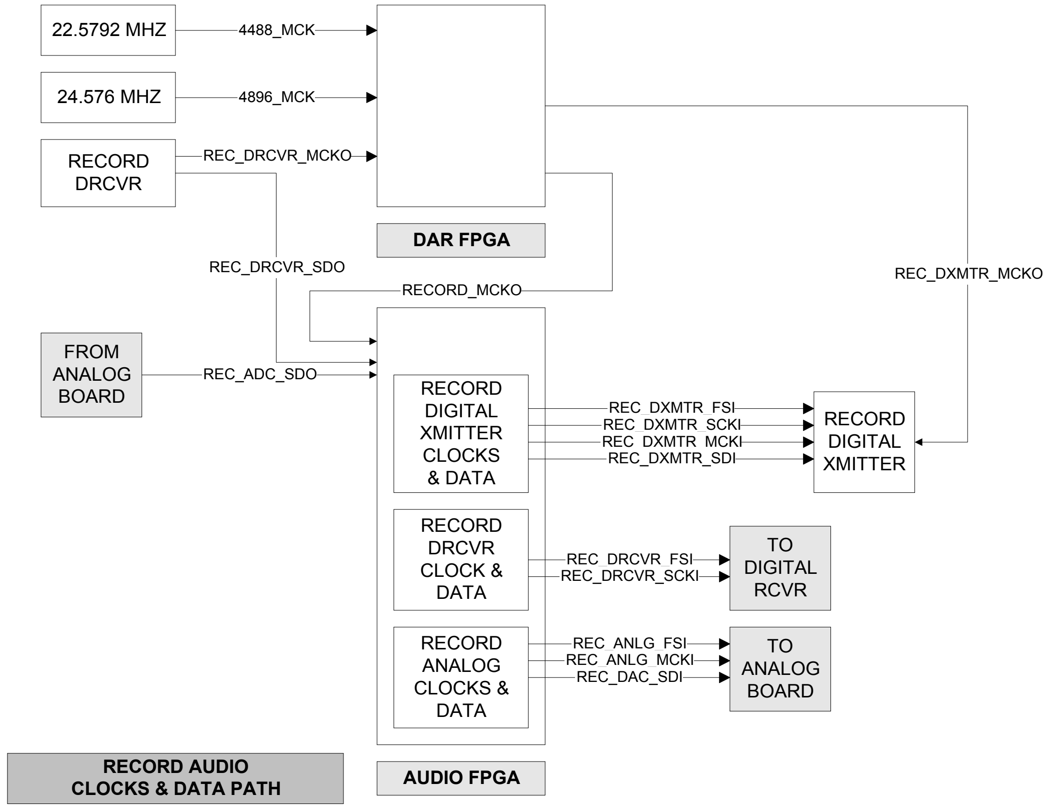


Record Audio Clock and Data Paths *(schematic pages 4 and 16 – 19)*

The Record Audio Data Path is as follows:
1. Output of the Record Digital Receiver and the Record ADC to the Audio FPGA
2. A 2-channel stream is sent to the Analog board as **REC_DAC_SDI** and to the Record Digital Transmitter as **REC_DXMTR_SDI**. This stream is either the output of the Record ADC, the Record Digital Receiver or a 2-channel down-mix of the Main Audio content.

There are three possible sources of master clock for the Record Audio Path. The 22.5792MHz crystal oscillator that provides either a 44.1kHz or 88.2kHz sample rate, the 24.576MHz oscillator that provides either a 48kHz or 96kHz sample rate, or the master clock output of the Record digital receiver. In practice, the unit runs off the crystal at 96kHz when the input is analog. When the input is digital, the master clock output of the digital receiver is used.
Depending on the input selected, the appropriate master clock is routed from the DAR FPGA to the Audio FPGA. Here it drives a clock tree that divides down the master clock, which is 256 times the sample rate, 256FS, to create the other clock rates required.

- The Digital Receiver uses a word clock, FS, and bit clock, 64FS.
- The Analog Board receives a 256FS Master Clock and a word clock, FS. These are used on the analog board to derive the audio clock signals required by the devices on that board.
- The Record Digital Transmitter requires an input master clock at 256FS, a bit clock at 64FS and an FS word clock. A separate output master clock is required by the sample rate converter section of the transmitter, which uses it to drive the output bitstream when the output sample rate is different from the input sample rate.



Zone 2 Audio Clock and Data Paths *(schematic pages 4 and 16 – 18)*

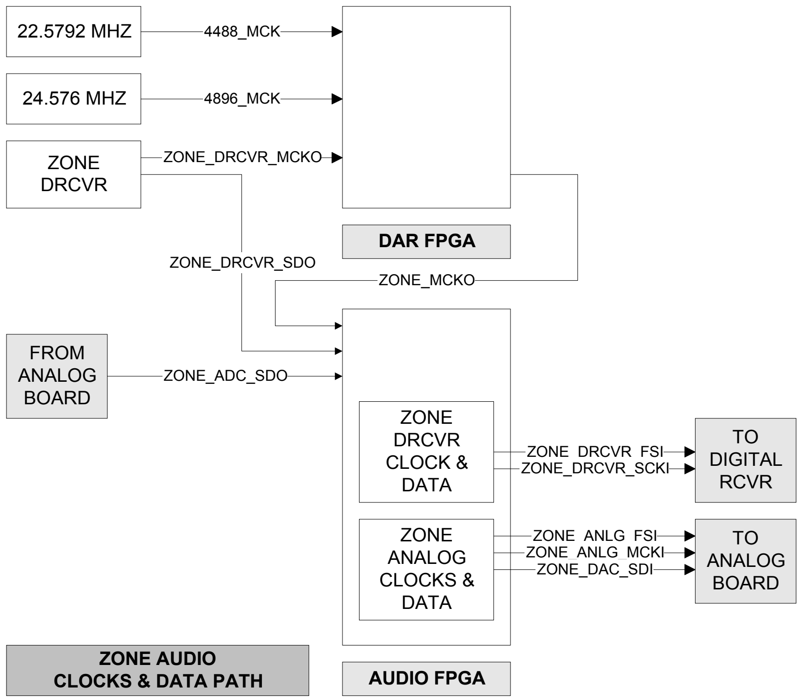
The Zone Audio Data Path is as follows:

1. Output of the Zone Digital Receiver and the Zone ADC to the Audio FPGA
2. A 2-channel stream is sent to the Analog board as **ZONE_DAC_SDI.** This stream is either the output of the Zone ADC, the Zone Digital Receiver or a 2-channel down-mix of the Main Audio content.

There are three possible sources of master clock for the Zone Audio Path. The 22.5792MHz crystal oscillator that provides either a 44.1kHz or 88.2kHz sample rate, the 24.576MHz oscillator that provides either a 48kHz or 96kHz sample rate, or the master clock output of the Zone digital receiver. In practice, the unit runs off the crystal at 96kHz when the input is analog. When the input is digital, the master clock output of the digital receiver is used.

Depending on the input selected, the appropriate master clock is routed from the DAR FPGA to the Audio FPGA. Here it drives a clock tree that divides down the master clock, which is 256 times the sample rate, 256FS, to create the other clock rates required.

- The Digital Receiver uses a word clock, FS, and bit clock, 64FS.
- The Analog Board receives a 256FS Master Clock and a word clock, FS. These are used on the analog board to derive the audio clock signals required by the devices on that board.



ENCODER

Encoder Processing (main board schematic sheet 1)

The two encoder signals ENCODER_A, ENCODER_B connect to inputs on the mem cpld U79. When either one is asserted low, the TRIGGER/ output is asserted, which discharges the CHARGE/ voltage on C243 through D42. TRIGGER/ remains asserted until CHARGE/ is sensed to have reached the low logic threshold of the cpld input. This guarantees that even brief signals from the encoder will discharge C243 sufficiently. When CHARGE/ drops below about 4V, the emitter of Q6 becomes reverse-biased, which asserts T_RUN/ low. When both encoder phases return high, C243 is allowed to charge through R263, delaying the rise of CHARGE/. If either encoder phase returns low before CHARGE/ reaches around 4V, another TRIGGER/ event is initiated, and the sequence restarts. When CHARGE/ finally is allowed to reach 4V, the emitter of Q6 becomes forward-biased and T_RUN/ returns high, ending the detection sequence. At that point, logic within U79 updates the internal 2-bit position reguster. Each complete T_RUN/ cycle corresponds to a single transition between detents, and direction is determined by whether ENCODER_A or ENCODER_B was the first phase asserted at the start of the cycle.

The timing circuit acts as a retriggerable one-shot multivibrator whose interval begins when both encoder phases have returned high. The time is chosen to be longer than the duration of expected sliding-contact dropouts. If both encoder phases are at a high level, that state could either represent a brief dropout or it could represent a legitimate detent state. Discriminating between the two is based on time. The time must not be too long, however, because legitimate transitions occur close together when the encoder is rotated rapidly. The time chosen for the MC-12 encoder is around 1msec and represents a good compromise between rejecting noise and accepting legitimate transitions.

The following figures illustrate the operation of the circuit.

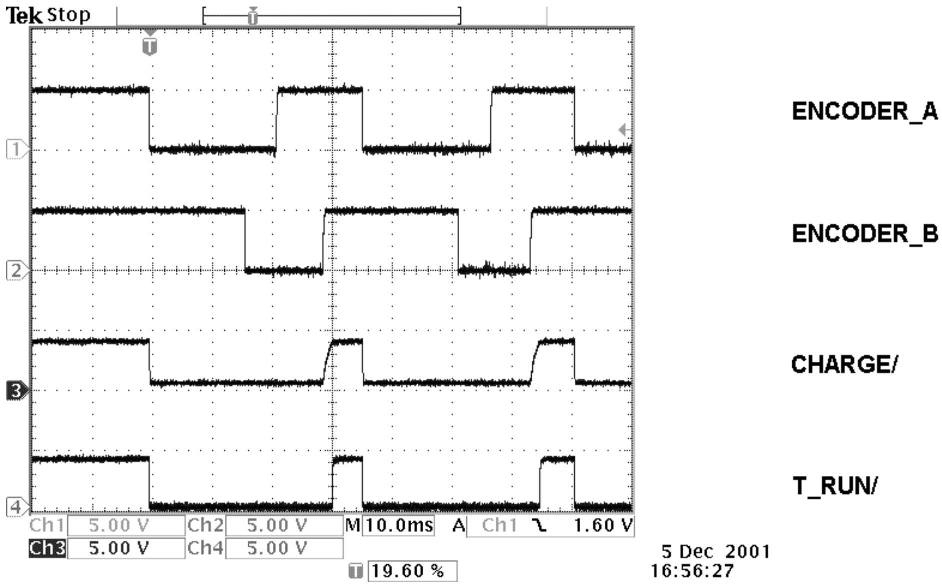


Figure 1. Normal Encoder

Figure 1 illustrates the operation of a new, well-behaved encoder. T_RUN can be seen to end at the delayed trailing edge of CHARGE/, which begins rising when ENCODER_B returns high. With opposite direction of rotatation, B would precede A.

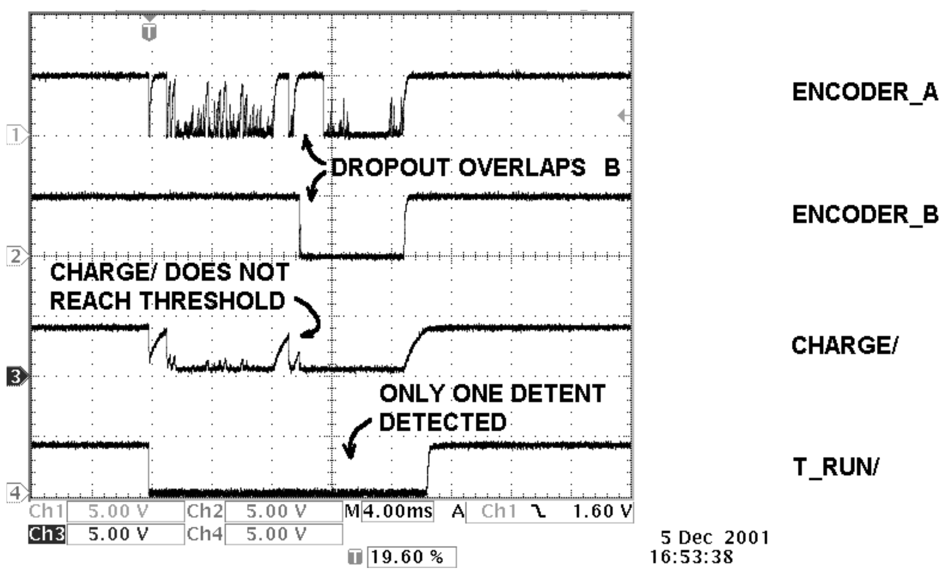


Figure 2. Noisy Encoder, Detail

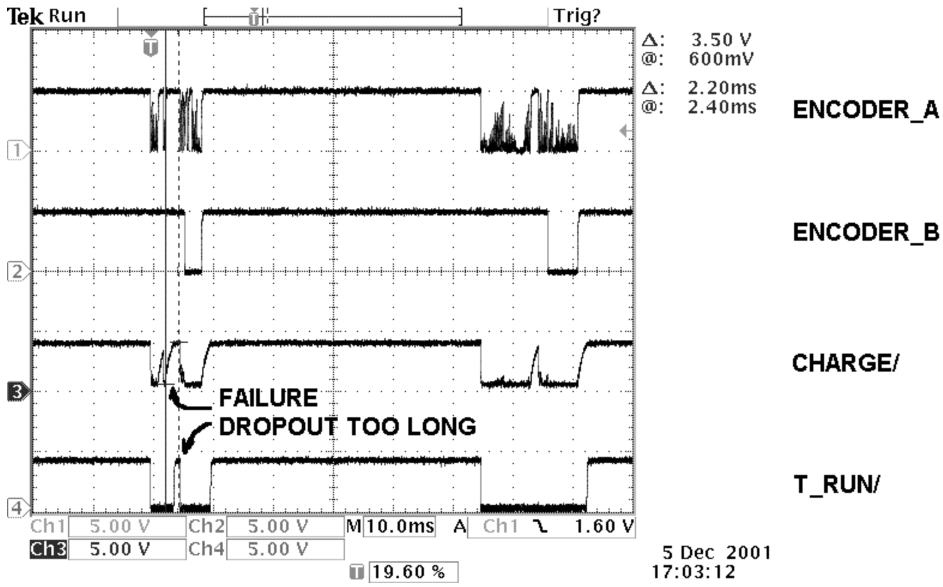


Figure 3. Defective Encoder

Figure 3 illustrates defective encoder operation. Dropout time exceeds 2msec (the manufacturer's spec), and two T_RUN cycles are seen during a single detent transition.

VCO BOARD OVERVIEW

The MC-12 VCO board (schematic 060-14849) is an isolated Voltage-Controlled Oscillator module that forms part of an overall Phase-Locked Loop (PLL) for generating master clocks for digital audio in the MC-12 system.

The board is housed in a shielded enclosure and mounts to the Main Board through a 5-pin in-line header J1, which carries control-voltage input, oscillator output, and 5-volt power and ground.

The VCO assembly is soldered to the MC-12 Main Board (schematic 060-13659), which incorporates the phase-detector and error amplifier to form the complete PLL.

VCO Circuit (VCO board schematic sheet 1)

U1 oscillates at a frequency determined by L1, C3, and the capacitance of varactor diode D1. L1 is a permeable-core inductor having high Q, necessary for oscillator purity. The tuning slug is factory set for a nominal 1uH inductance, and the operating range of the circuit is wide enough that no adjustment is necessary. A positive voltage on VCO_V of about 2VDC produces oscillation at about 17MHz, and 13VDC produces about 33MHz. A larger positive voltage increases the reverse bias of D1, lowering its capacitance and raising the resonant LC frequency. The cathode of D1 is effectively grounded for AC through bypass-capacitor C5. Series bead FB1 helps isolate the control point from spurious external influences. If VCO_V is much below 2V, D1 will become forward-biased; oscillation will stop and there will be no output.

The oscillator output is about 700mV p-p biased at around 3.5VDC, coupled through series-resistor R1 to help isolate the oscillator from load influences. External signal conditioning is necessary to convert the output OSC to a logic level that is compatible with downstream logic devices.

The VCO module is intended to be operated at 22.579MHz or 24.576MHz, with control voltage in the 5- to 6-Volt range.

VCO Signal Conditioning (main board schematic sheet 18)

The 700-mVpp OSC output of the VCO is ac-coupled and amplified to a 5V logic level by U44, which is self-biased near the middle of its inverting characteristic. The VCO module and associated sensitive circuitry is supplied from a dedicated 5V regulator (U32).

PLL OVERVIEW

The purpose of the PLL is to develop a pure, stable clock that matches the average properties of a potentially jittery, unstable reference. The elements of a PLL are frequency/phase detector, error amplifier/filter, and controllable oscillator.

PLL Phase Detector (main board schematic sheet 16)

PLL_MCKO from the VCO is fed to the DAR FPGA U19, for use as a 512FS master clock at 44/48kHz and a 256FS master clock at 88/96kHz. Within the FPGA, the VCO frequency is divided by 512, to 44 or 48kHz, and the result is frequency/phase-compared with a corresponding frequency derived from a selected reference (e.g. quartz crystal, digital audio receiver). When the frequency of the VCO is too low relative to the reference, a train of active-high pulses occurs on PLL_PUMP_UP. When the VCO frequency is too high relative to the reference, a train of active-low pulses occurs on PLL_PUMP_DOWN/.

PLL Error Amplifier / Filter (main board schematic sheet 18)

The non-inverting input of op-amp U45 is biased at 2.5V by a voltage divider from the regulated +5VA. The pump pulses from U19 are buffered by U33 and connect to schottky diodes D12,D13. When no pulses are asserted, the diodes are reverse-biased and no current is injected into the summing node of U45. When the VCO frequency is too low, D12 will be forward-biased by UP/ pulses asserted low by U33. The resulting current through R122 gets integrated by feedback capacitors C172 and C171 to produce progressively higher voltage at VCOV, which raises the VCO frequency. Conversely, DOWN pulses asserted high produce progressively lower voltage, lowering the VCO frequency. R125 damps the transient response of the loop. The integrator is the dominant element of the loop filter. The tendency of the closed loop is to adjust VCOV to synchronize the VCO frequency with the reference.

PLL Behavior in Lock (main board schematic sheet 18)

In lock, both of the pump pulses are inactive, and other circuitry determines the behavior of the loop. The loop enters a special state that produces high purity oscillation.

In lock, PLL_LOCK_DOWN/ delivers a train of low-going pulses at 44.1 or 48kHz whose average duty-cycle is designed to be about 1/128, independent of frequency. Instability or jitter in the reference will appear as variations in pulse width, but the instantaneous variation gets averaged by the action of the loop filter. The result is a steady control voltage that produces a high-stability VCO oscillation based on the average frequency of the reference.

The pulse duty-cycle is adjusted automatically by an additional branch in the feedback loop. When a pulse forward-biases D11, current flows through R120 and gets integrated by C167. R119 supplies a constant current of opposite polarity which also gets integrated. The two integrals oppose each other, and when the net current into the summing node is 0, the voltage at U45-1 remains effectively constant (DC). If the duty-cycle of the pulse is too small, the voltage is driven progressively lower, and vice-versa. The resulting voltage is applied to R121, which sinks current from the summing node of the loop integrator, which tends to raise VCOV. This tendency gets counteracted by current pulses through D14 and R124. When the integral of these two currents balance, VCOV remains constant, so OSC is a constant frequency, and the loop is locked.

D16 prevents VCOV from going much below 2V, to ensure that the VCO is never driven into a non-oscillating state. D15 prevents the duty-cycle integrator from being driven to the wrong polarity when the loop is out of lock.

The gain of the loop is such that the PLL_PUMP_UP and PLL_PUMP_DOWN/ pulses will cause the VCO frequency to change quickly when the loop is trying to achieve lock, based on R122, R123. When the phase comparator detects that the duty-cycle is < 1/64, the loop is considered to be in lock, and special gating logic within U19 disables the PLL_PUMP_DOWN/ pulse, so only PLL_LOCK_DOWN/ remains active. This greatly reduces the gain of the loop, based on R124. The reduced loop gain in lock means that the VCO frequency remains relatively insensitive to phase fluctuations (jitter) of the reference, yet when out of lock it can slew rapidly to track abrupt reference frequency changes, as when switching to a different sample rate.

When the PLL circuitry is not operating closed-loop, U45-1 drops to around –13V, and VCOV eventually rises to around +13V. Under these circumstances, the VCO oscillates at a poorly-controlled high frequency of 30MHz or higher.

Analog BOARD

OVERVIEW

The MC-12 Analog Board encompasses all of the analog audio inputs and outputs, level controls and A/D and D/A converters. This board is separate from and is located immediately above the MC-12 Main Board. All of the Digital Audio I/O connectors, transmitters and receivers are found on the Main board.

The MC-12 can be described as a complex audio switch matrix. There are three separate signal paths: Main, Record and Zone 2. Each of the 8 analog stereo inputs or 13 digital inputs can be routed to any or all of the three paths. The Main path digitizes the analog signal (if selected) and passes it to the DSP. *(Please refer to the Main Audio Path 2-Channel Input block diagram below)*. The DSP can create as many as 12 different output signals from the 2-channel input. Individual stereo D/A converter ICs operate in mono mode to convert each of the 12 signals from the DSP to analog. The signals pass through level controls and output drivers to their respective RCA connectors. A direct analog path is also provided which passes a 2-channel analog input signal directly to the Left and Right Front outputs via the level controls, bypassing the DSP and converters.

Error! Not a valid link.

The MC-12 Balanced version offers additional Balanced Main and Zone 2 analog outputs using XLR connectors. In this version, an internal 34 pin ribbon cable routes the post level control signals from the Analog Board to the XLR Board. The XLR Board incorporates active balanced output drivers for each of the 14 outputs.

In addition a 5.1 channel source can be selected for the Main audio path. There are four possible methods of getting a 5.1 source into the box. *(Please refer to the Main Audio Path 5.1-Channel Input block diagram below)*.

1. An S/PDIF signal may be encoded in Dolby Digital or DTS format and passed through a decoder that outputs the 5.1 channels. These channels are then passed along to the DSP.

2. Three separate analog input pairs can be routed directly to the outputs, bypassing the DSP and converters. This mode is available for DVD-Audio and multi-channel SACD players with 5.1 analog outputs. In this case, Input 6 would pass to the Left and Right Front outputs, Input 7 would pass to the Center and Mono Subwoofer as well as the Left and Right Subwoofer outputs. Input 8 would pass to the Left and Right Side and Rear outputs. In this case, Record and Zone 2 functionality is not restricted.

3. Three separate analog input pairs can be routed to the DSP by using the Record and Zone 2 input muxes and A/D converters. While this is engaged, the Record and Zone 2 paths cannot source analog inputs. This allows 5.1 analog inputs to be processed by the MC-12.

4. Three separate digital audio inputs with the same sample rate can be routed to the DSP by using the Record and Zone 2 input muxes and S/PDIF receivers. While this is engaged, the Record and Zone 2 paths cannot source digital audio inputs.

Error! Not a valid link.

Any of the 8 analog or 13 digital audio inputs can be selected as the source for the Record Audio Path. *(Please refer to the Record & Zone 2 Audio Paths block diagram below)*. An analog source can be passed directly to the analog outputs or be digitized and come out as an S/PDIF data stream. Likewise, a digital source can be sample-rate converted or passed directly to the digital outputs and be routed to a D/A converter for the analog outputs. In addition, a 5.1 Dolby Digital or DTS encoded 5.1 digital source may also be selected and passed through a decoder which will output a 2-channel downmix for the Record outputs. Two separate analog output pairs are provided, one with a fixed output level and the other with a variable output level for use as a 3rd Zone output. Two S/PDIF output ports are also available, one RCA (coax) and one Toslink (optical).

The Zone 2 Audio Path is similar to the Record Audio Path but does not have the S/PDIF outputs. A third stereo A/D converter and input level control have been designed in to permit selection of a 5.1-channel analog audio source for the Main Audio Path. Note this A/D section is not used for Zone 2 functionality and is not shown in the diagram.

Error! Not a valid link.

ANALOG AUDIO INPUTS

(schematic sheets 1 & 2)
Sheets 1 and 2 are identical. The Left input jacks and associated circuitry are on sheet 1, while sheet 2 includes the Right input jacks and circuitry. Each input pair is buffered by a dual TL072 op amp followed by a resistive divider that reduces the signal by 6 dB. Each buffer connects to three DG408 8x1 CMOS switches. There are separate switches for the Main, Record and Zone 2 analog source selection with independent switches for left and right channels, for a total of six DG408s.

The outputs of the Main source selectors feed the Main Input Level control on sheet 3, and two dual op amps on sheets 1 and 2. These op amps are used for the direct analog path to the Front L/R outputs. The first op amp is a unity gain voltage follower. The second amplifier inverts the signal and has 1.9 dB of gain.

At the bottom right-hand corner of each sheet are two op amps. These amplifiers are used when routing a 5.1 analog source. One routes the Center and Subwoofer signals from Input 7 while the other routes the Surround L/R signals from Input 8. Each inverting amplifier reduces the signal level by 4.4 dB.

MIC INPUTS AND MAIN A/D CONVERTER

(schematic sheet 3)
Up to four microphone inputs are provided on the MC-12 rear panel for future calibration features. A 10-pin connector provides the interface to a separate small board that holds the 1/8" microphone connectors and preamplifiers. *(This board is described later in this chapter.)* A DG411 analog switch can select either Mic inputs 1&2 (when MIC_SEL0 is high) or Mic inputs 3&4 (when MIC_SEL1 is high) to be passed to the Main Input level control and A/D converter. When a Mic input is selected, the Analog inputs are disabled by bringing MAIN_ANLG_EN low on sheets 1 and 2.

The Main Input level control is the CS3310, which has a range from +31.5 to –95.5 dB in 0.5 dB steps. The CS3310 operates on ±5 volt rails and cannot handle signal levels greater than 7.5 Vpp. Two dual op amps provide the left and right differential audio signals to the A/D converter. The op amp circuits bias the signals at 2.5 V and attenuate it by 7 dB. This means a 2 Vrms signal at the output of the level control will be equivalent to 0 dBFS after the A/D conversion.

The AK5383 stereo A/D converter incorporates a dual-bit delta-sigma architecture. It outputs 24 bits at a 96kHz sample rate under normal operation. The serial audio data from the A/D converter goes directly to the Main board. The A/D also provides a signal to mute the Main analog inputs (MAININ_VC_MUTE/) when it is going through calibration during power up or sample rate changes. Control signals are used for reset (MAIN_AD_RST/) and to place the converter in 88.2k or 96k sample rate mode (MAIN_AD_96K_EN). The Analog FPGA (sheet 17) provides three clocks: MAIN_AD_MCLK/, which is 256xFS for 44.1k and 48k sample rates, 128xFS for 88.2k and 96k sample rates; MAIN_AD_SCLK/, which is 64xFS; and MAIN_AD_LRCK/ which is 1xFS (where FS = sample rate).

RECORD AND ZONE 2 A/D CONVERTERS

(schematic sheet 4)

The Record and Zone 2 Input level controls and A/D converter circuits are identical to what is used by the Main inputs, which are described in the Main A/D Converter section. The selected analog source gets routed to the CS3310 level control. Dual op amps condition the signal for the A/D converters with 2.5 V of bias and 7 dB of attenuation. Again, a 2 Vrms signal at the output of the level control will be equivalent to 0 dBFS after the A/D conversion.

Note that the Zone 2 Input level control and A/D converter are not required for the Zone 2 path because there is no associated digital output. The Zone 2 A/D converter and level control is only used when an analog 5.1 channel source needs to be processed.

RECORD AND ZONE 2 D/A CONVERTERS

(schematic sheets 5 & 6)

Sheets 5 and 6 are identical with one minor difference on the Zone 2 output at the lower right hand corner. The Record path is on sheet 5 and Zone 2 path on sheet 6.

The AK4395 24-bit delta-sigma stereo D/A converter operates up to 192 kHz. Each DAC is configured through its serial control port (pins 8,10,11) with a separate Reset pin.

The output of the DAC passes through a 3rd order low pass filter with its –3 dB frequency at 100 kHz. The filter topology is a compromise between the flat passband Butterworth filter and the Bessel filter with its superb transient response. The filter is pretty much flat out to 20 kHz. It has an overall gain of 1.4 dB when measured at the test points. This means a 0 dBFS signal at the D/A converter will be 2 Vrms going into the analog switches.

DG411 analog switches select either the output of the respective DAC or the analog input source directly for the Record or Zone 2 outputs. The selected signal goes off to sheet 7 to the fixed-level outputs and to the on-page CS3310 output level control. Both Record and Zone 2 have two sets of analog outputs. One set is labeled “Fixed” and has a maximum output level of 4 Vrms that cannot be varied. The other set is labeled “Variable” and has an associated level control to vary the output level. The “Fixed” outputs provide a unity gain path through the MC-12 for Record and Zone 2 analog inputs.

After the signal passes through the CS3310, it is boosted by 6 dB by a non-inverting op amp and then goes off to sheet 7. The one schematic difference is the muting relay for the variable output is shown on sheet 6 for Zone 2; the respective relay for the Record variable output is shown on sheet 7.

RECORD AND ZONE 2 OUTPUTS

(schematic sheet 7)

The Record outputs are located in the upper half of sheet 7; Zone 2 outputs in the lower half.

The Record variable-level outputs from sheet 5 come in on the left hand side of the schematic and pass through a muting relay before going to the output jacks. The fixed-level outputs come into non-inverting stages with 6 dB of gain to insure unity gain for analog input sources. These signals also pass through a

muting relay on the way to the output jacks. The relays for both the fixed and variable-level outputs operate in parallel and are controlled by the RECOUT_MUTE/ signal.

The Zone 2 variable-level outputs from sheet 6 come in on the left hand side of the schematic and go directly to the output jacks. As in the Record path, the fixed-level outputs come into non-inverting stages with 6 dB of gain to insure unity gain for analog input sources. These signals pass through a muting relay on the way to the output jacks. The relays for both the fixed and variable-level outputs operate in parallel and are controlled by the ZON2OUT_MUTE/ signal on sheet 6.

MAIN D/A CONVERTERS

(schematic sheets 8-13)

There are 12 outputs for the Main Audio Path. The D/A circuitry is shown for two outputs on each sheet. The circuitry is identical for all twelve outputs.

The AD1853 is a stereo multi-bit delta-sigma 24-bit D/A converter that operates at sample rates up to 192 kHz. Each D/A IC is configured in mono mode. This means there are two D/A converters being used to provide each of the MC-12's twelve outputs. By doing so, this topology insures the best performance in terms of high-level THD and dynamic range.

The Analog FPGA (sheet 17) is the source for the clocks and data for the D/A converters. The data is manipulated in the FPGA to create an inverted copy of the DAC's left channel data for its right channel, necessary to operate the DACs in mono mode.

The MCLK, SCLK and LRCK clocks are distributed from the Analog FPGA (sheet 17). The MCLK is at 256x the sample rate (FS) and is inverted and distributed independently for each DAC pair. The SCLK (64xFS) and LRCK (1xFS) are distributed to three sets of four DACs via separate source resistors. All of the D/A converters operate in I^2S mode.

The AD1853 DACs are configured through their serial ports (pins 3,4,5). FRONT_DAC_RST/ puts the Front L/R pair of DACs into reset, while all other DACs share the same reset line (MAIN_DAC_RST/).

The AD1853 has current outputs. The combined currents OUTL+ and OUTR- are fed to one summing node of a dual op amp which acts as a current-to-voltage (I/V) converter. Similarly, OUTL- and OUTR+ are fed to the other summing node. The non-inverting inputs are biased at about 2.7V by the FILTR pin of the AD1853.

The I/V converter produces a differential voltage from the combined D/A current outputs. Each current-output pin sinks a bias of 1mA, and delivers full-scale signal current of +/-0.75mA around that bias point (0.25 to 1.75 mA). The output voltage at the I/V converter is determined by its feedback resistor (6.49k). For example, the full-scale AC signal voltage developed due to OUTL+ would be +/-(0.75mA*6.49k) = +/-4.9V; it becomes +/-9.8V when the equal contribution of OUTR- is added.

A separate DC feedback scheme is used to eliminate DC bias from the outputs of the I/V converters. The feedback loop is formed by 2N3904 and 2N3906 transistors and their associated passive components. The 2N3906 supplies bias currents into the summing nodes via two resistors, while the 2N3904 senses the sum of the I/V converters outputs. The objective of this circuit is to maximize the voltage range available for the audio signal, thus improving the signal-to-noise ratio. By eliminating DC bias in the output of the I/V converters, their full-scale AC signal voltage is +/-9.8V.

The current outputs from the DACs have substantial components at frequencies well above the audio band, and the combination of series ferrite beads, across-the-line capacitor, and feedback caps in the I/V converters are important for reducing this high-frequency content.

The DAC's I/V converters are followed by a 3rd order low pass filter. The filter topology is a compromise between the flat passband Butterworth filter and the Bessel filter with its superb transient response, with the –3 dB point at 90 kHz and the passband flat to 20 kHz. The filter attenuates the 17Vpp differential signal to 6.8Vpp (2.4Vrms) and converts it to single-ended for the level controls. Note these values assume a 0 dBFS digital input signal to the DAC.

In all of the output channels except for Aux, DG411 analog switches are used to select either the DAC output or analog input for the respective output. These direct analog signal paths have been designed in to support two modes:

1. 2-channel analog direct or bypass mode. Any analog input can be routed directly to the L/R Front outputs.
2. 5.1-channel analog direct or bypass mode. When this mode is enabled, specific analog input signals are routed to specific analog outputs according to the table below:

Analog Input	Analog Output(s)
#6, left channel	Left Front
#6, right channel	Right Front
#7, left channel	Center
#7, right channel	Mono Sub, Left & Right Subs
#8, left channel	Left Side and Left Rear
#8, right channel	Right Side and Right Rear

Two different pairs of control bits are used to select the DSP/DAC signals or analog input signals for the Main outputs. FRONT_DACOUT_SEL/ selects the Front L/R DAC outputs for the Left and Right Front outputs when low. FRONT_DIRECT_SEL/ selects the analog input for the Front outputs. MAIN_DACOUT_SEL/ selects the respective DAC outputs for all of the other Main outputs (Center, Mono Sub, L/R Sub, L/R Side, L/R Rear) whereas MAIN_DIRECT_SEL/ selects the 5.1 analog inputs directly.

MAIN OUTPUTS

(schematic sheets 14-16)
Sheets 14, 15 and 16 are identical, with each sheet including four of the twelve Main output circuits. One of the circuits is described below.

The output from the analog switch goes to a CS3310 output level control. This level control operates from +/-5V rails with a gain range from +31.5 to –95.5 dB in 0.5 dB steps. Each CS3310 controls a signal pair.

The outputs from the level control feed a dual op amp. Each op amp is configured as an inverting amplifier with 10.4 dB of gain. The output signals pass through DC-blocking caps and relays before going to the RCA connectors. The relays mute the Main outputs during a power cycle and whenever the unit is in Standby or Off. Three separate 2N4401 transistors are used to drive four relays each to minimize the stress on the transistor.

The CS3310 outputs also go to a 34-pin connector on sheet 19. This connector is used for routing the audio to the XLR board in MC-12 Balanced models.

ANALOG FPGA

(schematic sheet 17)
A Xilinx 144-pin FPGA is the "brains" behind the analog board. Its purpose in life includes:

- 3 internal clock trees for the Main, Record and Zone 2 A/D and D/A converters
- Provides independent outputs for A/D and D/A converter clocks
- Realigns and buffers the audio data for all D/A converters
- Serial state machine that allows the Z180 to control the DACs and level controls serially
- Provides the chip selects for 7 control registers

The Z180 on the Main board communicates to the FPGA via an 8-bit data (DBA_D[7:0]) and 5-bit address (DBA_A[4:0]) bus. Appropriate Read (DBA_RD/), Write (DBA_WR/) and Chip select (DBA_CS/) signals are active during communication.

The Main clock tree comes into the FPGA with a Master clock (MAIN_ANLG_MCK) and word clock (MAIN_ANLG_FS). Data for the Main DACs (MAIN_DAC_SD[5:0]) comes into the FPGA in I^2S format relative to the word clock input. The FPGA reclocks the data internally and reformats it to support the "mono mode" operation of the Main DACs. Each DAC receives its own data serially from the FPGA. Separate clocks are provided for the Main A/D converter and Main D/A converters. The following tables provide a description of the Main clock and data I/O:

Main Inputs	Description
MAIN_ANLG_MCK	Master clock input (256FS)
MAIN_ANLG_FS	Word clock input (FS)
MAIN_DAC_SD0	Front L/R DAC I^2S data
MAIN_DAC_SD1	Center/LFE DAC I^2S data
MAIN_DAC_SD2	Sub L/R DAC I^2S data
MAIN_DAC_SD3	Side L/R DAC I^2S data
MAIN_DAC_SD4	Rear L/R DAC I^2S data
MAIN_DAC_SD5	Aux L/R DAC I^2S data

Analog FPGA – Main Clock and Data Inputs

Main A/D & D/A Outputs	Description
MAIN_AD_MCLK/	A/D Master clock (128FS@96k)
MAIN_AD_SCLK/	A/D Serial data clock (64FS)
MAIN_AD_LRCK/	A/D Word clock (FS)
MAIN_DAC_ MCLK/	D/A Master clock (256FS)
MAIN_DAC_ SCLK/	D/A Serial data clock (64FS)
MAIN_DAC_ LRCK/	D/A Word clock (FS)

Analog FPGA – Main A/D & D/A Clock Outputs

Likewise, the Record and Zone 2 converters have independent clock trees so they can each run at different sample rates than the Main channels. The data for the D/A converters is reclocked inside the FPGA. The following tables provide a description of the Record and Zone clock and data I/O:

Record Inputs	Description
REC_ANLG_MCK	Master clock input (256FS)
REC _ANLG_FS	Word clock input (64FS)
REC _ANLG_SDI	Record DAC I^2S data

Analog FPGA – Record Clock and Data Inputs

Record Outputs	Description
REC _AD_MCLK/	A/D Master clock (128FS@96k)
REC _AD_SCLK/	A/D Serial data clock (64FS)
REC _AD_LRCK/	A/D Word clock (FS)
REC _DAC_ MCLK/	D/A Master clock (256FS)
REC _DAC_ SCLK/	D/A Serial data clock (64FS)

REC _DAC_ LRCK/	D/A Word clock (FS)
REC _DAC_ DATA	D/A I^2S data

Analog FPGA – Record Clock and Data Outputs

Record Inputs	Description
ZON2_ANLG_MCK	Master clock input (256FS)
ZON2 _ANLG_FS	Word clock input (64FS)
ZON2 _ANLG_SDI	Zone 2 DAC I^2S data

Analog FPGA – Zone 2 Clock and Data Inputs

Record Outputs	Description
ZON2 _AD_MCLK/	A/D Master clock (128FS@96k)
ZON2 _AD_SCLK/	A/D Serial data clock (64FS)
ZON2 _AD_LRCK/	A/D Word clock (FS)
ZON2 _DAC_ MCLK/	D/A Master clock (256FS)
ZON2 _DAC_ SCLK/	D/A Serial data clock (64FS)
ZON2 _DAC_ LRCK/	D/A Word clock (FS)
ZON2 _DAC_ DATA	D/A I^2S data

Analog FPGA – Zone 2 Clock and Data Outputs

CONTROL REGISTERS AND MAIN BOARD CONNECTOR

(schematic sheet 18)

Seven discrete 74HC273 control registers are located on the board. The Z180 writes to them via the 8-bit data bus (DBA_D[7:0]). The decoding for the chip selects resides in the Analog FPGA.

Control Register 0 provides the following:

- Mute relay control for the Main RCA outputs (MAINOUTS_MUTE/)
- Mute relay control for the Main XLR outputs (EXPOUTS_MUTE/)
- Mute relay control for the Record fixed and variable RCA outputs (RECOUT_MUTE/)
- Mute relay control for the Zone fixed and variable RCA & XLR outputs (ZON2OUT_MUTE/)

Control Register 1 provides the following:

- Analog source selection for the Main audio path (MAIN_ANLG_SEL[2:0]; MAIN_ANLG_EN)
- Main A/D calibration and 96kHz sample-rate enable (MAIN_AD_RST/; MAIN_AD_96K_EN)

Control Register 2 provides the following:

- Analog source selection for the Record audio path (REC_ANLG_SEL[2:0]; REC_ANLG_EN)
- Record A/D calibration and 96kHz sample-rate enable (REC_AD_RST/; REC_AD_96K_EN)

Control Register 3 provides the following:

- Analog source selection for the Zone 2 audio path (ZON2_ANLG_SEL[2:0]; ZON2_ANLG_EN)
- Zone 2 A/D calibration and 96kHz sample-rate enable (ZON2_AD_RST/; ZON2_AD_96K_EN)

Control Register 4 provides the following:

- Independent Zero crossing enable for each Main output level control (FRONT_VC_ZCEN, etc.)
- Zero crossing enable for the Record output level control (RECOUT_VC_ZCEN)
- Zero crossing enable for the Zone 2 output level control (ZON2OUT_VC_ZCEN)

Control Register 5 provides the following:
- Record DAC reset control (REC_DAC_RST/)
- Record output selection – DSP or analog direct path (REC_DACOUT_SEL/; REC_DIRECT_SEL/)
- Mute for Record output level control (RECOUT_VC_MUTE/)
- Zone 2 DAC reset control (ZON2_DAC_RST/)
- Zone 2 output selection – DSP or analog direct path (ZON2_DACOUT_SEL/; ZON2_DIRECT_SEL/)
- Mute for Zone 2 output level control (ZON2OUT_VC_MUTE/)

Control Register 6 provides the following:
- Main DACs reset control (MAIN_DAC_RST/)
- Main outputs selection – DSP or analog direct path (MAIN_DACOUT_SEL/; MAIN_DIRECT_SEL/)
- Mute for Main output level controls (MAINOUT_VC_MUTE/)
- Front Main DACs reset control (FRONT_DAC_RST/)
- Front Main output selection – DSP or analog direct path (FRONT_DACOUT_SEL/; FRONT_DIRECT_SEL/)
- Mute for Front Main output level control (FRONT_VC_MUTE/)

Also shown on sheet 18 is a 60-pin dual row ribbon connector, the interface to the Main board.

XLR BOARD CONNECTOR, POWER SUPPLY CONNECTIONS AND REGULATORS

(schematic sheet 19)
A 26-pin dual row ribbon connector routes the audio signals to the XLR board for MC-12 Balanced models.

There are two separate feeds from the 90W switching power supply to the Main and Analog boards. The Video board gets its power from the analog board. The Analog board has a 6-pin connector that accepts ±15 volts, ±5 volts and two ground connections to the supply. A 4-pin connector supplies the Video Board with +5VD, +5VA and –5VA.

A 7805 voltage regulator creates the +5VA supply from the +15V rail. Heat is dissipated by a heatsink and a 10 ohm, 5W power resistor. +5VA is an alternative “clean” 5 volt supply used by the A/D and D/A converters and other sensitive circuitry.

XLR BOARD OVERVIEW

The MC-12 Balanced XLR output board (schematic 060-14469) provides balanced versions of the 12 main audio outputs and the two variable Zone 2 audio outputs. Input signals and power are connected through a 34-pin ribbon cable to the Analog I/O board. The XLR board is housed in its own chassis, which attaches to the basic MC-12 chassis to form the complete MC-12 Balanced.

MAIN CHANNELS

(XLR board schematic sheets 1,2).
Specific references are to the left front channel; other main channels are similar. LFRONT+ is the unbalanced audio driven by volume control chip U37 on the Analog I/O board, fed through a series 100-ohm resistor and the ribbon cable, connecting to the XLR Board at J15-4. FRONTRTN connects through the cable to the signal ground near the driving point. Op-amp U21 and associated circuitry amplify the difference between LFRONT+ and FRONTRTN with a gain of 3. The combination of R62 and the 100-ohm resistor at the driven end matches the value of R60, preserving differential symmetry and giving high common-mode rejection. FRONTRTN is a ground-sense line dedicated to the front channel pair. The differential stage with remote ground-sensing rejects common-mode ground differences that arise between boards due to ir drops in the common ground connections.

U14 is a balanced audio line-driver with nominal open-circuit gain of 6.7dB and low output impedance, capable of driving 600-ohm loads. It also has high output common-mode rejection, so its differential output

tends to be independent of any imbalance in output loading. Its outputs are AC-coupled through non-polar electrolytic capacitors C109,C110. With a 600-ohm load, the AC-coupling gives a lower, -3dB frequency of around 10Hz.

Relay RY14 mutes the left front output through its normally-closed contacts in un-powered and un-controlled situations. Q2 energizes the relay and un-mutes when EXPOUTS_MUTE/ is set high by software.

The XLR Board has an overall inverting characteristic. When LFRONT+ is negative-going, pin 2 of J14 is positive-going. This matches the inversion occurring in the final unbalanced output stage on the Analog I/O Board, so the RCA and XLR outputs are in-phase. The overall gain is such that the open-circuit level at each balanced main output is approximately twice that of its unbalanced counterpart.

ZONE 2 VARIABLE CHANNELS

(XLR board schematic sheet 3).

The description of the main channels applies to the zone-2 channels, with the following exceptions.

The differential stage, U15, has a gain of 2. The final unbalanced output stage on the analog i/o board is non-inverting, so the zone-2 RCA and XLR outputs will be seen to be out-of-phase. The overall gain is such that the open-circuit level at each balanced zone-2 output is approximately 2.16 times that of its unbalanced counterpart. The driver transistor for the zone-2 mute relays RY1, RY2

OPTO/MIC INPUT BOARD

This is a small helper board which has low-level microphone preamplifiers and optical inputs. The outputs from the microphone preamps are sent to the Analog Board via a ribbon cable and eventually to the A/Ds on that board. The optical inputs are sent via another ribbon cable to the Main Board.

Microphone Preamplifiers

The circuitry here supplies power (9 volts) to an external microphone capsule, and performs balanced to unbalanced conversion and amplification. The input op-amp is protected from the common-mode phantom power by 10uF input capacitors and an inductor capacitor RFI filter network. The op-amp has unity gain to a differential signal from the microphone while rejecting common-mode noise. The output of the op-amp is amplified by nineteen by the next op-amp. A 270 ohm resistor isolates the output from reactive loads.

Microphone "Phantom" Power Supply

Power is pulled from the +15 supply and regulated down to 9 volts by a voltage regulator. Diode D1 prevents back-biasing the regulator when +15 is removed. An RC filter is created by 330 ohms and 10uF. The 2.2K resistors provide current limiting and define the input impedance that the microphone sees at the input of the amplifier.

Optical Inputs

This part of the board serves as a riser board for three optical S/PDIF inputs. Power is supplied by the Main Board via a separate cable.

Video BOARD

OVERVIEW

The MC-12 video section consists of two major functional blocks: video switcher and on-screen display generator (OSD).

The video assembly consists of two boards, the Video RCA Board, schematic 060-13609, and the Video Board, schematic 060-13679.

The two boards are interconnected with a flexible 32-pin ribbon connector, with most of the active circuitry contained on the Video Board. Video input and output connectors are mounted directly on the boards, which attach to the rear panel of the MC-12. Separate cables supply power and control signals to the video assembly. Control from the Main Board is implemented via a serial interface.

COMPOSITE VIDEO INPUTS

(Video RCA board schematic sheet 1)
Specific references are to input 1; other inputs are similar. Standard video levels applied to RCA jack J18 develop 1Vp-p across 75-ohm termination resistor R17. Emitter-follower Q7 is located close to the connector and buffers the input with a gain slightly less than unity. Transistor bias is supplied through R16 only when the channel is selected by control lines MVID_SEL or RVID_SEL which operate CMOS switches U1 and U2. DC power from the -5V rail is applied to the emitter resistor through the on-resistance of the switch, which is only a few tens of ohms. Buffers without bias are effectively disabled, so an on-board video transmission path is subject to crosstalk from at most one other simultaneously active (hostile) composite video input. Buffered video is fed to pin 27 of ribbon cable J22 through low-value series resistor R15, which reduces high-frequency peaking in the transmission path to the Video Board.

COMPOSITE VIDEO OUTPUTS

(Video RCA board schematic sheet 1)
Composite video outputs originating on the Video Board are fed through individual pins of J22 to the corresponding output RCA jacks. The on-board traces are controlled-impedance and form part of a 75-ohm wideband transmission system, and output level is 1Vp-p when terminated in 75 ohms (2Vp-p open-circuit).

S-VIDEO INPUTS

(Video board schematic sheet 1)
Specific references are to input 1; other inputs are similar. S-video luminance inputs (pin 4 of the mini-DIN jacks) are terminated and buffered the same as composite inputs. AC-coupling is applied after buffering; C59 couples S-video input 1, C167 couples composite input 1. Chrominance input 1 (pin 3 of mini-DIN jack J18) is first ac-coupled by C22, and then buffered by emitter follower Q20. The DC-level at the chroma input pin is direct-coupled to subsequent sense circuitry through R54. Bias to the luma/chroma emitter-follower pairs is controlled by U6/U7.

MONITOR COMPOSITE / S-VIDEO

(Video board schematic sheet 2)
Composite and S-video luminance connect to multiplexers U9, U25, and S-video chrominance connects to U10. The monitor-channel multiplexers are addressed by the MVID-SELn bits. When MCVID_EN/ is asserted low, U25 is enabled and the multiplexer selects one composite source. The opposite sense enables U9 and U10 for selecting one S-video source. Q24 is a simple inverter. The composite/luminance (MY) signal from U9/U25 is amplified by non-inverting stage U23. R156 makes the gain be slightly greater than the desired factor of two in order to make up for slight losses in other stages. The signal from U23-1 is fed through R155 to the sync-stripper and DC-restorer (sheet 7). The DC-correction signal BPCOR returns through R158 to close the DC-feedback loop and maintain the video back-porch near 0VDC. The signal OSD_Y_IN is distributed to output amplifiers U15, U14, U39, U38, and also feeds the on-screen display (sheet 5).

Chroma selected by U10 (MC) is ac-coupled by C102 and amplified by U23, also with gain slightly greater than two. With a composite source selected, U10 is disabled, no signal is selected, and the chroma channel is turned off. D6 is used to enhance chroma on/off switching. With U10 disabled, D6 is forward-biased by R152, shunting the un-driven node with a low impedance to ground. When U10 is enabled, the DC level at

U10-3 is negative due to the operating point of the selected emitter-follower, D6 is reverse-biased and is effectively an open circuit. The signal OSD_C_IN is distributed to output amplifiers U22, U14, U39, U38, and also feeds the on-screen display (sheet 5).

The DC-level on the chroma channel of the selected source is fed to the base of Q22 through multiplexer U8 and the associated 100k series resistor. R95 raises the threshold for sensing a high level. The DC-amplifier formed by Q22 and Q21 is disabled when MORPHEN/ is high. When enabled, a high DC-level on the chroma input will drive base current into Q22. Q22 saturates and turns on Q21, which applies a high DC-level to the filter formed by R92 and C49. With low DC-level input, both transistors remain off, and no DC is fed to the filter. This circuit discriminates a low or high DC voltage on the selected chroma input and forms a 0 or 5V level accordingly. Sensing threshold is around 3V.

For both composite video and S-video, there are two monitor outputs available. The On-Screen Display (OSD) feature is available on the MONITOR 1 outputs, but is absent from the MONITOR 2 outputs.

Monitor 1 S-video at J4 is driven by gain-of-one amplifiers U15 (luma) and U22 (chroma). Internal multiplexers in these amplifiers determine whether the video is taken from the OSD path (MTHRU/=hi) or straight through from the input amplifiers (MTHRU/=low). Amplifier outputs are fed through 75-ohm series resistors (R121, R148), forming a matched transmission-line driver system. R120 and R147 compensate for slight impedance errors due to the resistance of the on-board connecting traces. The chroma output is AC-coupled by C76, with a DC-level introduced through R2. When MORPHEN1/ is asserted low, switch U21 permits the Monitor 1 chroma output to follow the DC-sensing circuit.
Monitor 2 S-video at J3 is driven by gain-of-one amplifiers in U14, which are always driven from the input amplifiers. R119 and R116 are required by the current-amplifier topology of U14. Output impedance and coupling is structured as with Monitor 1. When MORPHEN/=low, the chroma DC-level of the selected input is sensed and replicated on the Monitor 2 chroma output through R1.

Monitor 1 composite video CVID_MON1 is driven by U39. Luma and chroma from the input amplifiers are summed by R199 and R200, scaled by 1/2. The result is amplified by U39, which has a gain of slightly more than two. With composite input, there is no chroma, and the result is simply the composite video. With S-video input, the result is the composite version of the S-video, the sum of Y+C. As with the S-video monitor 1 path, the internal U39 multiplexer selects whether the OSD is in the path or whether the input is fed straight through, controlled by MTHRU/. Output impedance is structured as with the Monitor 1 luma output.

Monitor 2 composite video CVID_MON2 is driven by U38 and is always taken directly from the input amplifiers, bypassing the OSD. Summing, gain, and output are as described for Monitor 1.

Standard 1Vp-p video input levels produce 1Vp-p output on the composite and luminance channels when terminated in 75 ohms, or 2Vp-p open circuit. The composite monitor outputs are fed to RCA jacks on the Video RCA Board via ribbon cable J25.

RECORD COMPOSITE / S-VIDEO

(Video board schematic sheet 3)
Record video circuitry is structured similarly to monitor video, but without OSD capability. Refer to the previous section for additional description. Multiplexers U16, U24, and U17 are addressed by the RVID_SELn bits to select an independent record source, but otherwise operate like their counterparts in the monitor path. There is no DC-restorer in the record path, so back-porch DC-level varies with average picure level due to input ac-coupling. The two sets of record outputs are driven by common output amplifiers through separate series-terminating resistor paths. The multiplexer internal to U27 allows the record S-video luminance to be shut off when a composite source is in use. The record monitor outputs are fed to RCA jacks on the Video RCA board via ribbon cable J25.

COMPONENT VIDEO SWITCHER

(Video RCA board schematic sheet 2, Video board schematic sheet 3)

Component video switching is performed by high-bandwidth relays to maximize signal fidelity and format compatibility. There is no active circuitry in the component video path.

Three sets of component input RCA jacks (component inputs 1,2,3) are mounted on the video RCA board and feed a 3-wide, two-tier tree of DPDT relays. The tree selects one of the input sets to be transmitted to the Main Board via 75-ohm coaxial jumpers J19,20,21. One transistor driver is associated with each set of 3 relays. Relays are actuated when the associated PSELn bit is asserted high, switching from the normally-closed to the normally-open circuits.

One set of component input BNC jacks (component input 4) is mounted on the Video Board. A set of 3 relays (RY3,4,7) forms another tier of the relay tree and selects either input 4 or the set fed from the RCA board via J19,20,21. RY6 permits the selected luminance to be routed through the OSD via buffer Q4. The final tier of the tree (RY1,2,5) connects the output BNC jacks either to the selected component source or to the OSD. Relays are actuated through their driver transistors when the associated PSELn bit is asserted high.
Note: component video overlays are not implemented in current operating system software.

Component OSD luminance (Y) is taken from the normal analog luminance output of the OSD chip. Color-difference signals (Pr, Pb) are derived from logic-level signals from the RGB port of the chip. U19 buffers the logic levels and provides inverted versions of R and B. A resistor array forms a weighted sum of the RGB levels along with appropriate DC-offset and scaling to implement the standard color-difference matrix:

$$Y=.587G+.299R+.114B$$
$$Pr = .713 (R-Y)$$
$$Pb =.564 (B-Y).$$

U11 serves as buffer/filter/output driver for the Pr and Pb and drives the outputs through series-terminating resistors R101, R105.

The signals generated by the MC-12 OSD are compatible only with the 480i component format. When incompatible formats are in use, the component OSD is inapplicable, and is not accessed by the operating system software.

ON-SCREEN DISPLAY SIGNALS

(Video board schematic sheet 5)
OSD chip U34 produces a character-based video display that can be overlaid on program video or that can occupy a full-screen, based on an independent internal video generator. OSD modes and parameters are controlled by an extensive set of internal registers, accessed via serial interface.

The character strings to be displayed are loaded serially into the screen memory within the chip. The bitmapped patterns that define the shapes of individual characters are stored in external font memory, interfaced through the A[18:0] and D[7:0] buses (see below). Character dot-clock is fixed at about 15 MHz, based on the external LC circuit formed by L18/C140/C139. A crystal clock is supplied by oscillator U35 (PAL) or U36 (NTSC). The active oscillator is determined by a high level on either NTSC_EN or PAL_EN, enabling the respective oscillator.

In overlay mode, composite or S-video luminance from the input amplifier is applied to YIN, and similarly, S-video chrominance (if applicable) is applied to CIN. The video applied to YIN is shifted to have a back-porch DC-level of about 1.57VDC by U13 and associated circuitry. C97/C75 passively couple the ac-content of the luminance signal, with the op-amp providing the DC response. The chroma channel is biased to the same 1.57V level by R201/R202. The OSD video is related to program video by the separate H and V syncs (GMHSYN/, VSYNC/) derived by the sync stripper (sheet 7).

The full-screen mode is independent of video and sync inputs. Raster generation is based on the appropriate crystal clock.

The OSD luminance output is DC-shifted back to 0V back-porch level by U13 and associated circuitry. C141/C142 passively couple the AC-content, with the op-amp providing the DC response. Chroma is simply ac-coupled by C149/C150. The shifted OSD video is buffered and filtered by U37 to produce OSD_SY_OUT and OSD_SC_OUT. OSD_PY_OUT is buffered separately by U38 to drive the component OSD luminance output. Switch U21 permits the S-video luminance to be turned off when MSVID_OFF is asserted high. OSD_Y+C_OUT is formed as half the sum of the buffer outputs. These OSD output signals feed the output amplifiers as described earlier.

In order to produce usable overlays in the SECAM system, the OSD switching action is bypassed at high frequency through U21 and R144, preserving an attenuated version of the FM color carriers.

SUPPORT LOGIC / FPGA

(Video board schematic sheet 6)
When power is applied, the video FPGA receives its configuration program from SROM U29. Once configured, the FPGA interfaces the Main Board serial control port to the Video Board.

There are 3 possible destinations for control data on the Video Board: OSD, control registers, and character font SRAM. Data are conveyed in multiple 8-bit packets on VIDEO_DATA, accompanied by VIDEO_SCLK, operating at 1 MHz.

Data and clock connect directly to the OSD chip U34, and when chip-select OSD/ is asserted from the Main Board, the FPGA asserts OSD_CS/ to implement the interface to the chip. Each logical transfer to the OSD chip consists of a pair of single-byte transfers.

VIDEO_REG/ acts as a multi-purpose chip-select that supports data transfer to other subsystems of the Video Board.

To access the video control registers (sheet 8), VIDEO_REG/ is asserted and 3 bytes of data are sent while VIDEO_REG/ remains low. VREG_DATA is clocked into the shift stages of U3,4,5 by the rising edge of VREG_SCLK. When VIDEO_REG returns high, logic within the FPGA generates a special strobe, VREG_RCLK, to transfer data from the internal stages to the output latches of the chips. The FPGA synchronizes VREG_RCLK with VSYNC/ so that latching occurs during vertical blanking. In the absence of sync, the strobe will occur by default after a several tens of milliseconds, using the 15kHz clock as a timebase. If VIDEO_REG/ returns high after only one byte of serial data, the byte gets latched into a register implemented within the FPGA, and no external strobe gets generated.

The FPGA recognizes one register bit as a command to enter a special mode for initializing the character font SRAM (U31,32,33). In this mode, the host keeps VIDEO_REG/ asserted while it sends the font pattern bytes to fill the SRAMs. Logic within the FPGA converts the received serial bytes to parallel, drives the A[18:0] and D[7:0] buses, and asserts WR/, generating write cycles to transfer data to the SRAMs. It takes over over a second to complete the transfer, and during this time the OSD A and D buses are tri-stated with OSD_TSC/ asserted low. Once loaded, the OSD chip accesses the SRAMs and fetches 3 bytes of pattern data for each character, for a total of 3x24 reads on every active horizontal scan line.

SYNC STRIPPER / DC RESTORER

(Video board schematic sheet 7)
Video from input amplifier U23 is fed through R155 to the series LC chroma trap formed by L17 and associated capacitors. With NTSC_EN asserted, U12 connects directly to C91, disconnecting C90 and making the LC trap frequency about 3.6MHz. With the switches in the other position, the effective capacitance is the series combination of C90 and C91, and the resulting lower capacitance raises the trap frequency to about 4.4MHz, suitable for PAL. Trapping the chroma enhances the accuracy of back-porch DC-restoring. U20 buffers the chroma trap output and drives sync stripper U1 and the DC-restorer formed by switch U12 and op amp U20.

Sync stripper U1 accepts analog video and extracts vertical and horizontal sync, producing logic level VSYNC-OUT and AFC-OUT pulses respectively. A phase-locked loop based on ceramic resonator Y1 provides robust horizontal sync extraction even from noisy video sources. Pull-down resistors on the outputs improve the pulse waveshapes. Sections of U2 buffer and shape the pulses from U1. AFC-OUT is stretched by R69/C1 before buffering in order to meet the minimum width necessary for the OSD chip. Sections of U2 and the network formed by R71,R72,D1 and C36 form pulses that are aligned with video back porch. These pulses switch U12, which in combination with integrator U20 forms a sample-and-hold circuit that closes the feedback loop around the input video amplifier during back-porch time. This acts to maintain the back-porch level at 0V. D5 limits the negative-going output of U20 in order to minimize the undesirable effects of unusual sync patterns inherent in the macrovision video copy-protection scheme.

Additional logic within U1 detects the presence of a valid video input. SYNC_DETECT is fed to the Main Board for use in OSD management.

With video input absent, AFC_OUT free-runs at around 15kHz, and is used as a general purpose clock to govern some default timing of state machines within the FPGA.

VIDEO CONTROL REGISTERS

(Video board schematic sheet 8)
U3,4, and 5 are 8-bit shift registers which are cascaded to receive a 24-bit word. Each chip contains internal shift stages plus a set of output latches. The shift clock and data are arbitrated by the FPGA, as described earlier. Data that has been accumulated in the shift stages gets transferred simultaneously to all 24 output latches when the FPGA strobes the VREG_RCLK. All control bits are initialized to 0 at power-up. VIDEO_RST/ is asserted to clear the internal shift stages. When reset is removed, the FPGA generates a special VREG_CLK to transfer the internal zeros to the output latches. This occurs after a default interval based on the 15kHz clock.

POWER AND CONTROL INTERFACE

(Video board schematic sheet 9)
J24 is the control and status interface to the host. J22 supplies power from a connector on the analog board. The main video +5-volt rail is +5VV, a filtered version of system +5VD, which also supplies relay coils through FB2. The negative rail is -5VV, derived from the analog board -5VA. The sync stripper U1 is specially-powered from a well-regulated rail, +5VAS, derived from the Analog Board +5VA.

Chapter 7 - Parts List

MC-12/MC-12 Balanced MAIN BOARD

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
202-09794	RESSM,RO,0 OHM,0805	11.00		R81-84,90-93,109 R157,282
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	8.00		R1,16,18,20,22,24 R26,246
202-09871	RESSM,RO,5%,1/10W,1K OHM	7.00		R2,241,242,247,263 R283,287
202-09873	RESSM,RO,5%,1/10W,10K OHM	34.00		R28,29,56,111,137 R138,140,141,144-151 R175,232,244,248,255 R267-274,278,279,286 R296,297
202-09874	RESSM,RO,5%,1/10W,2.2M OHM	2.00		R119,121
202-09894	RESSM,RO,5%,1/10W,1M OHM	1.00		R152
202-09897	RESSM,RO,5%,1/10W,470 0HM	4.00		R31,76,80,280
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	17.00		R3-6,65,133,135,136 R139,142,143,195,238 R243,249,256,257
202-10558	RESSM,RO,5%,1/10W,47K OHM	9.00		R15,17,19,21,23,25 R117,118,245
202-10559	RESSM,RO,5%,1/10W,100 OHM	3.00		R128,295,298
202-10571	RESSM,RO,5%,1/10W,100K OHM	1.00		R251
202-10836	RESSM,RO,5%,1/4W,1K OHM	6.00		R32,33,38,39,43,44
202-10890	RESSM,RO,5%,1/10W,220 OHM	24.00		R112-115,129-132 R252-254,284,285 R288-294,300-303
202-10944	RESSM,RO,5%,1/10W,33K OHM	1.00		R134
202-10946	RESSM,RO,5%,1/10W,3.3K OHM	1.00		R299
202-10949	RESSM,RO,5%,1/10W,1.2K OHM	3.00		R122,123,125
202-11071	RESSM,RO,5%,1/4W,75 OHM	7.00		R7-12,36
202-11496	RESSM,RO,0 OHM,1206	31.00		R48,49,54,55,59,61 R77,78,89,98,176 R207,208,212,218,229 R233-237,239,240 R258-262,264-266
202-12365	RESSM,RO,5%,1/4W,110 OHM	1.00		R27
202-14792	RESSM,RO,5%,1/10W,56 OHM	110.00		R13,14,30,50,51,57 R58,60,62,64,66-75 R79,85-88,94-97 R101-107,110,116 R153-156,158-174 R177-194 R196-206,209-211 R213-217,219-228 R230,231,275,277
203-10424	RESSM,RO,1%,1/10W,4.99K OHM	2.00		R126,127
203-10896	RESSM,RO,1%,1/10W,1.00K OHM	4.00		R37,42,47,250
203-11733	RESSM,RO,1%,1/10W,3.57K OHM	3.00		R34,40,45
203-11741	RESSM,RO,1%,1/10W,18.2K OHM	1.00		R120
203-12167	RESSM,RO,1%,1/10W,374 OHM	1.00		R53
203-12363	RESSM,RO,1%,1/10W,90.9 OHM	1.00		R52
203-12722	RESSM,THIN,1%,1/10W,49.9K OHM	1.00		R124
203-13131	RESSM,RO,1%,1/10W,8.45K OHM	3.00		R35,41,46
240-09786	CAP,ELEC,100UF,25V,RAD,LOW ESR	2.00		C257,264

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
240-10758	CAPSM,ELEC,1UF,50V,20%,5.5MMH		2.00	C171,243
240-12330	CAPSM,ELEC,2.2UF,35V,20%	2.00		C185,241
240-13216	CAPSM,ELEC,22UF,16V,20%	3.00		C45,47,49
240-13217	CAPSM,ELEC,47UF,16V,20%	3.00		C170,172,181
240-13803	CAP,ELEC,560UF,35V,RAD,LOW ESR	1.00	06/11/01■	C267
241-09798	CAPSM,TANT,10UF,10V,20%	3.00		C123,163,256
241-11799	CAPSM,TANT,4.7UF,6.3V,20%	7.00		C43,75,90,179,184 C187,189
244-10423	CAP,MYL,.22UF,50V,RAD,5%,BOX	2.00		C252,253
244-11589	CAP,MYL,.068UF,63V,RAD,5%,BOX	3.00		C41,73,88
245-09105	CAPSM,CER,.027UF,50V,X7R,10%	48.00		C92-115,125-148
245-09291	CAPSM,CER,470PF,50V,COG,5%	2.00		C183,240
245-09876	CAPSM,CER,.01UF,50V,Z5U,20%	9.00		C13,16,17,20,21 C24,27,261,262
245-10562	CAPSM,CER,150PF,50V,COG,10%	9.00		C3-9,251,254
245-10588	CAPSM,CER,33PF,50V,COG,10%	11.00		C2,14,15,18,19,22,23 C25,26,191,192
245-11595	CAPSM,CER,.01UF,50V,COG,5%	1.00		C182
245-11645	CAPSM,CER,.47UF,50V,Z5U,20%	3.00		C46,48,50
245-12485	CAPSM,CER,.1UF,25V,Z5U,20%	152.00		C1,10-12,28-40,42,44 C51-72,74,76-87,89 C91,116-122,124 C149-154,157-162 C164-169,173-178,180 C186,188,190,193-239 C242,244-250,255 C258-260,263
270-11545	FERRITESM,CHIP,600 OHM,0805	15.00		FB1-13,15,16
270-13802	INDUCTORSM,24UH,20%,2.74A	1.00	06/11/01■	L1
300-10509	DIODESM,1N914,SOT23	5.00		D15,16,27,31,42
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	8.00		D1-8
300-10564	DIODESM,SCHOTTKY,LOW VF,SOT23	5.00		D11-14,26
300-11599	DIODESM,GP,1N4002,MELF	5.00		D9,10,21,28,29
310-10510	TRANSISTORSM,2N3904,SOT23	2.00		Q2,3
310-10565	TRANSISTORSM,2N3906,SOT23	3.00		Q1,4,6
310-10566	TRANSISTORSM,2N4401,SOT23	1.00		Q5
330-09241	ICSM,DIGITAL,74HCT574,SOIC	2.00		U42,48
330-09889	ICSM,DIGITAL,74ACT04,SOIC	1.00		U33
330-10523	ICSM,DIGITAL,74HCU04,SOIC	5.00		U2-4,44,52
330-12452	ICSM,DIGITAL,74VHCT244,SOIC	9.00		U55,62-64,68,70-72 U86
330-13865	ICSM,DIGITAL,74VHC04,SOIC	2.00		U26,49
330-13866	ICSM,DIGITAL,74VHC244,SOIC	1.00		U51
330-13868	ICSM,DIGITAL,74VHC574,SOIC	4.00		U41,47,56,57
330-13876	ICSM,DIGITAL,74VHC273,SOIC	4.00		U40,46,53,83
330-13882	ICSM,DIGITAL,74LCX14,SOIC	1.00		U38
330-14247	ICSM,DIGITAL,74VHCT245,SOIC	7.00		U59-61,69,73-75
330-14534	ICSM,DIGITAL,74VHCT541,SOIC	5.00		U9,21,28,54,84
340-09244	ICSM,LINEAR,78LS05,5V REG,SOIC	1.00		U32
340-10567	ICSM,LIN,MC34164,+5V MON,SOIC	1.00		U77
340-11597	ICSM,LIN,TL072,DUAL OPAMP,SOIC	1.00		U45
340-13137	IC,LINEAR,LM2941CT,ADJ,TO-220	3.00		U10-12
340-13883	ICSM,LIN,LM2937,2.5V REG,TO263	1.00		U43
340-14535	IC,LIN,1585A,3.3V REG,TO220	1.00		U82
345-12038	ICSM,INTER,75ALS180,DR/RC,SOIC	1.00		U5
345-13138	ICSM,INTER,CS8414,RCVR,SOIC	3.00		U8,20,27
345-13139	ICSM,INTER,CS8420,ASRC,SOIC	1.00		U17
345-13140	ICSM,INTER,RS232 XCVR,+5V,SOIC	1.00		U1
350-12456	ICSM,SRAM,128KX8,12NS,3.3V,SOJ	8.00		U13-16,22-25
350-13676	ICSM,CPLD,MC12,MEM,V1.00	1.00		U79
350-13854	ICSM,FPGA,XCS05XL-4,10X10,VQFP	2.00		U19,67

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
350-13863	ICSM,SRAM,32KX8,70NS,SOIC,20UA	1.00		U76
350-13879	ICSM,SDRAM,512KX32X4,3.3V,TSOP	2.00		U31,36
350-14540	ICSM,FPGA,XCS20XL-4,20X20,PQFP	1.00		U66
350-14784	IC,ROM,27C020,MC12,MAIN,V1.00	1.00		U58
365-13860	ICSM,UPROC,ADSP21065,60MHZ,PQF	4.00		U29,30,34,35
365-13861	ICSM,UPROC,Z8S180,33MHZ,PQFP	1.00		U80
365-13862	ICSM,UPROC,CS49326,DD/DTS,PLCC	1.00		U50
365-14683	ICSM,UPROC,PIC16C54,MC12,V1.00	1.00		U85
390-13864	RESONATOR,CER,4.00MHZ,.5%,5MM	1.00		Y1
390-13885	CRYSTAL OSCSM,29.491MHZ,TRI	1.00		U81
390-13886	CRYSTAL OSCSM,30.0MHZ,TRI,3.3V	1.00		U39
390-14543	CRYSTAL OSCSM,22.5792MHZ,TRI3V	1.00		U6
390-14544	CRYSTAL OSCSM,24.576MHZ,TRI,3V	1.00		U7
430-10419	LEDSM,INNER LENS,RED	6.00		D18,20,23,25,43,45
430-10420	LEDSM,INNER LENS,YEL	6.00		D30,33,35,37,39,41
430-10421	LEDSM,INNER LENS,GRN	11.00		D17,19,22,24,32,34 D36,38,40,44,46
460-04598	BATTERY,LITH,3V@160MAH,HORIZ	1.00		BAT1
470-12913	XFORMER,PULSE,AES,1:1,.2X.4SP	1.00		TX1
490-02356	CONN,JUMPER,.1X025,2FCG	6.00		W1-6 PINS 1&2
500-03620	CONN,EURO,C,ROW A+C,FEM	3.00		J23-25
500-13643	CONN,EURO,C,48P,ABC,RECP,VERT	1.00		J39
510-02899	CONN,POST,100X025,HDR,3MC	6.00		W1-6
510-03550	CONN,DSUB,9FC,PCRA,4-40THD INS	2.00		J3,4
510-03922	CONN,POST,100X025,HDR,6MCG	1.00		J36
510-03989	CONN,POST,156X045,HDR,2MCG,LOK	1.00		J32
510-10546	CONN,POST,079,HDR,4MC	1.00		J33
510-10595	PHONE JACK,3.5MM,PCRA,3C,STER	1.00		J1
510-10745	CONN,POST,100X025,HDR,2MC,POL	1.00		J30
510-12999	CONN,POST,.100,HDR,2X30MCG,LK	1.00		J29
510-13145	CONN,POST,.100,HDR,2X7MCG,LP	1.00		J26
510-13148	CONN,RCA,PCRA,1FCGX2V,BLK,GND	3.00		J6-8
510-13538	CONN,RCA,PCRA,1FCG,BLK,GND	1.00		J2
510-13840	CONN,OPTO,PCRA,TORX173,6MBPS	2.00		CP3,4
510-13873	CONN,HDR,.200,6MC,PCRA	1.00		J5
510-13887	CONN,POST,.100,HDR,2X13MCG,POL	1.00		J35
510-14079	CONN,POST,156X045,HDR,4MC,LOK	1.00		J31
510-14796	CONN,XLR,3FC,PCRA,LATCH,METSHL	1.00		J9
510-14833	CONN,OPTO,PCRA,XMTR,13.2MBPS	1.00		CP1
510-14835	CONN,OPTO,PCRA,RCVR,OMJ,8MBPS	1.00		CP2
520-04999	IC SCKT,32 PIN,MACH,TIN	1.00		U58
635-14671	SPCR,PCB,4-40X5/8,.219RD,STEEL	2.00		OPTO/MIC
640-01701	SCRW,4-40X1/4,PNH,PH,ZN	2.00		LUG1(DSUB CONN GND); U82 REG TO H/S
701-09640	BRACKET,KEYSTONE,621,4-40X2	1.00		LUG1 (DSUB CONN GND)
704-06165	HEATSINK,TO220,.75X.5X.5,TAB	3.00		U10-12
704-14452	HEATSINK,TO220,MTTAB,NUT,1.45H	1.00		U82

MC-12/MC-12 Balanced OPTO/MIC BOARD

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	8.00		R11,12,21,22,31,32 R38,39
202-09871	RESSM,RO,5%,1/10W,1K OHM	1.00		R44
202-09899	RESSM,RO,5%,1/10W,47 OHM	3.00		R1-3
202-10598	RESSM,RO,5%,1/10W,330 OHM	4.00		R13,23,33,40
202-11073	RESSM,RO,5%,1/4W,270 OHM	4.00		R8,18,28,42
203-11077	RESSM,RO,1%,1/10W,237 OHM	1.00		R45
203-11980	RESSM,THIN,1%,1/10W,10.0K OHM	16.00		R4-7,14-17,24-27

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
				R34-37
203-12481	RESSM,RO,1%,1/10W,1.5K OHM	1.00		R46
203-12719	RESSM,THIN,1%,1/10W,2.00K OHM	4.00		R9,19,29,41
203-12723	RESSM,THIN,1%,1/10W,102 OHM	4.00		R10,20,30,43
240-11827	CAPSM,ELEC,10UF,16V,20%	13.00		C3,10-12,20-22 C30-32,40-42
240-13216	CAPSM,ELEC,22UF,16V,20%	1.00		C46
245-10562	CAPSM,CER,150PF,50V,COG,10%	8.00		C13,14,23,24,33 C34,43,44
245-10976	CAPSM,CER,47PF,50V,COG,5%	12.00		C5,6,9,15,16,19,25 C26,29,35,36,39
245-12485	CAPSM,CER,.1UF,25V,Z5U,20%	13.00		C1,2,4,7,8,17,18 C27,28,37,38,45,47
270-11545	FERRITESM,CHIP,600 OHM,0805	8.00		FB1-8
300-11599	DIODESM,GP,1N4002,MELF	2.00		D1,2
340-10552	ICSM,LIN,MC33078,DU OPAMP,SOIC	4.00		U1-4
340-11559	ICSM,LIN,LM317M,+ADJ REG,DPAK	1.00		U5
510-10595	PHONE JACK,3.5MM,PCRA,3C,STER	4.00		J2-5
510-13840	CONN,OPTO,PCRA,TORX173,6MBPS	3.00		CP1,2,3A
680-14081	CABLE,100,PLUG/SCKT,2X5C,12"L	1.00		OPTO (J6) TO ANLG BD
680-14170	CABLE,RIB,24-26AWG,6CX.1,3"L	1.00		OPTO (J1) TO MAIN BD

MC-12/MC-12 Balanced VIDEO BOARD

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
202-09871	RESSM,RO,5%,1/10W,1K OHM	23.00		R7,8,14,15,21,22,28 R29,35,36,42,43,49 R50,56,57,69,73-75 R77,92,143
202-09873	RESSM,RO,5%,1/10W,10K OHM	10.00		R1,2,61,64,67,72,93 R94,176,179
202-09874	RESSM,RO,5%,1/10W,2.2M OHM	1.00		R142
202-10426	RESSM,RO,5%,1/10W,15K OHM	15.00		R80,82-84,96-98,114 R118,120,147,173,175 R198,206
202-10571	RESSM,RO,5%,1/10W,100K OHM	17.00		R5,12,19,26,33,40,47 R54,66,126,127,131 R146,151,152,158,187
202-10573	RESSM,RO,5%,1/10W,470K OHM	16.00		R76,85-91,99,122,145 R207-211
202-10943	RESSM,RO,5%,1/10W,22K OHM	3.00		R60,68,70
202-10944	RESSM,RO,5%,1/10W,33K OHM	5.00		R95,212-215
202-10945	RESSM,RO,5%,1/10W,1.5K OHM	1.00		R62
202-10947	RESSM,RO,5%,1/10W,680K OHM	1.00		R59
202-10948	RESSM,RO,5%,1/10W,390 OHM	1.00		R63
202-11042	RESSM,RO,5%,1/10W,6.8K OHM	4.00		R160,161,163,166
202-12369	RESSM,RO,5%,1/10W,36K OHM	4.00		R124,129,149,156
202-13579	RESSM,RO,5%,1/10W,22 OHM	17.00		R6,9,13,16,20,23,27 R30,34,37,41,44,48 R51,55,58,78
203-10560	RESSM,RO,1%,1/10W,75.0 OHM	32.00		R3,4,10,11,17,18,24 R25,31,32,38,39,45 R46,52,53,79,101 R105,115,117,121,148 R159,162,164,165,172 R174,191,197,205
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	4.00		R132,135,136,139
203-10837	RESSM,RO,1%,1/10W,475 OHM	7.00		R71,116,119,144,155 R169,192
203-10840	RESSM,RO,1%,1/10W,750 OHM	16.00		R102,103,123,125,128 R130,150,153,154,157

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
				R170,171,183,186,195
				R196
203-10895	RESSM,RO,1%,1/10W,681 OHM	2.00		R180,188
203-11080	RESSM,RO,1%,1/10W,1.15K OHM	10.00		R167,168,182,184,185
				R190,193,194,199,200
203-11082	RESSM,RO,1%,1/10W,15.0K OHM	1.00		R137
203-11723	RESSM,RO,1%,1/10W,4.75K OHM	5.00		R106,108,111,113,201
203-11726	RESSM,RO,1%,1/10W,301 OHM	2.00		R203,204
203-11730	RESSM,RO,1%,1/10W,1.37K OHM	2.00		R133,134
203-12198	RESSM,RO,1%,1/10W,2.15K OHM	5.00		R107,109,110,112,202
203-12298	RESSM,RO,1%,1/10W,30.1K OHM	1.00		R65
203-12838	RESSM,RO,1%,1/10W,29.4K OHM	1.00		R140
203-12897	RESSM,RO,1%,1/10W,976 OHM	4.00		R100,104,181,189
203-14789	RESSM,RO,1%,1/10W,61.9K OHM	1.00		R141
203-14790	RESSM,RO,1%,1/10W,11.8K OHM	1.00		R138
240-09786	CAP,ELEC,100UF,25V,RAD,LOW ESR	3.00		C115,116,120
240-10758	CAPSM,ELEC,1UF,50V,20%,5.5MMH	1.00		C25
240-11111	CAPSM,ELEC,47UF,6V,NONPOL,20%	15.00		C40,51-59,163-167
240-11827	CAPSM,ELEC,10UF,16V,20%	8.00		C31,104,117-119,142
				C150,160
240-13217	CAPSM,ELEC,47UF,16V,20%	3.00		C88,97,114
245-09291	CAPSM,CER,470PF,50V,COG,5%	1.00		C90
245-09876	CAPSM,CER,.01UF,50V,Z5U,20%	1.00		C72
245-09895	CAPSM,CER,10PF,50V,COG,10%	1.00		C139
245-10416	CAPSM,CER,1000PF,50V,COG,5%	3.00		C32,33,102
245-10544	CAPSM,CER,220PF,50V,COG,5%	2.00		C28,36
245-10561	CAPSM,CER,100PF,50V,COG,5%	2.00		C26,94
245-10972	CAPSM,CER,.068UF,50V,X7R,20%	1.00		C29
245-10975	CAPSM,CER,3300PF,50V,X7R,10%	1.00		C30
245-10976	CAPSM,CER,47PF,50V,COG,5%	3.00		C64,69,146
245-10977	CAPSM,CER,330PF,50V,COG,5%	1.00		C35
245-11625	CAPSM,CER,33PF,50V,COG,5%	1.00		C155
245-12070	CAPSM,CER,15PF,50V,COG,10%	1.00		C140
245-12485	CAPSM,CER,.1UF,25V,Z5U,20%	110.00		C1-24,27,34,37-39
				C41-50,60-63,66,67
				C70,71,73-87,89,92
				C93,95,96,98-101,103
				C105-113,121-138,141
				C143,144,149,151
				C152,156-159,161
245-12524	CAPSM,CER,68PF,50V,COG,5%	1.00		C148
245-14762	CAPSM,CER,6.8PF,50V,COG,5%	1.00		C153
245-14763	CAPSM,CER,12PF,50V,COG,5%	4.00		C65,68,145,147
245-14764	CAPSM,CER,82PF,50V,COG,5%	1.00		C154
245-14765	CAPSM,CER,180PF,50V,COG,5%	1.00		C91
270-00779	FERRITE,BEAD	4.00		FB1-4
270-11289	INDUCTORSM,10UH,10%	2.00		L17,18
300-10509	DIODESM,1N914,SOT23	2.00		D1,7
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	1.00		D5
300-10564	DIODESM,SCHOTTKY,LOW VF,SOT23	1.00		D6
300-11599	DIODESM,GP,1N4002,MELF	3.00		D2-4
310-10510	TRANSISTORSM,2N3904,SOT23	20.00		Q4-20,22-24
310-10565	TRANSISTORSM,2N3906,SOT23	1.00		Q21
310-10566	TRANSISTORSM,2N4401,SOT23	3.00		Q1-3
330-09797	ICSM,DIGITAL,74AC04,SOIC	1.00		U19
330-10505	ICSM,DIGITAL,74HC02,SOIC	1.00		U2
330-10506	ICSM,DIGITAL,74HC595,SOIC	3.00		U3-5
340-10502	ICSM,LIN,LF353,DUAL OPAMP,SOIC	2.00		U13,20

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
340-11495	ICSM,LIN,LT1229,VID OPAMP,SOIC	7.00		U11,14,18,23,26
				U37,38
340-13856	ICSM,LIN,EL4421C,VIDAMP,W/MUX	3.00		U15,22,27
340-14791	ICSM,LIN,EL4422C,VIDAMP,W/MUX	1.00		U39
345-10503	ICSM,INTER,NJM2229,SYNSEP,SOIC	1.00		U1
346-10507	ISCM,SS SWITCH,74HC4051,SOIC	9.00		U6-10,16,17,24,25
346-10508	ICSM,SS SWITCH,74HC4053,SOIC	2.00		U12,21
350-13921	ICSM,FPGA,XCS05-3,10X10,PLCC	1.00		U30
350-14248	ICSM,SRAM,128KX8,70NS,SOIC	3.00		U31-33
350-14785	IC,SPROM,MC12,VIDEO,V1.00	1.00		U29
365-13288	ICSM,UPROC,MB90092,OSDC,PQFP	1.00		U34
390-10516	RESONATOR,CER,503KHZ	1.00		Y1
390-13857	CRYSTAL,OSCSM,14.31818MHZ,TRI	1.00		U36
390-13858	CRYSTAL,OSCSM,17.73448MHZ,TRI	1.00		U35
410-13859	RELAY,1P2T,5V,DIP,MINI,RF	7.00		RY1-7
510-13128	CONN,MINIDIN,4FC,PCRA,GND	12.00		J1-4,11-18
510-13891	CONN,BNC,1FCG,PCRA,75 OHM	6.00		J5-10
510-14079	CONN,POST,156X045,HDR,4MC,LOK	1.00		J22
520-00941	IC SCKT,8 PIN,LO-PRO	1.00		U29
620-14766	LUG,SOLDER,.52IDX.66ODX.33H,TB	6.00		J5-10
680-14855	CABLE,100,PLUG/SCKT,2X7C,6"L	1.00		VIDEO(J24)TO MAIN BD

MC-12/MC-12 Balanced VIDEO RCA BOARD

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
202-09871	RESSM,RO,5%,1/10W,1K OHM	7.00		R1,2,4,7,10,13,16
202-13579	RESSM,RO,5%,1/10W,22 OHM	5.00		R3,6,9,12,15
203-10560	RESSM,RO,1%,1/10W,75.0 OHM	5.00		R5,8,11,14,17
240-11827	CAPSM,ELEC,10UF,16V,20%	2.00		C12,13
240-13217	CAPSM,ELEC,47UF,16V,20%	1.00		C1
245-12485	CAPSM,CER,.1UF,25V,Z5U,20%	14.00		C2-11,14-17
300-11599	DIODESM,GP,1N4002,MELF	2.00		D1,2
310-10510	TRANSISTORSM,2N3904,SOT23	5.00		Q3-7
310-10566	TRANSISTORSM,2N4401,SOT23	2.00		Q1,2
346-10507	ISCM,SS SWITCH,74HC4051,SOIC	2.00		U1,2
410-13859	RELAY,1P2T,5V,DIP,MINI,RF	6.00		RY1-6
510-13147	CONN,RCA,PCRA,1FCG,YEL,GND	9.00		J1-4,14-18
510-14545	CONN,RCA,PCRA,1FCG,RED,GND	3.00		J6,9,12
510-14546	CONN,RCA,PCRA,1FCG,GRN,GND	3.00		J7,10,13
510-14547	CONN,RCA,PCRA,1FCG,BLU,GND	3.00		J5,8,11
680-14856	CABLE,COAX,TERMINAL,4"L	3.00		J19-21
680-14857	CABLE,FFC,32CX.1,CRMP,ST/RA,3"	1.00		J22 (TO VIDEO BD)

MC-12/MC-12 Balanced ANALOG I/O BOARD

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
202-09794	RESSM,RO,0 OHM,0805	32.00		R157,159,163,164,179
				R180,191,192,198,199
				R205,206,212,213,219
				R220,226,227,236,237
				R243,244,250,251,326
				R335,411,415,419,572
				R574,575
202-09872	RESSM,RO,5%,1/10W,33 OHM	21.00		R546-558,562-565,567
				R569-571
202-09873	RESSM,RO,5%,1/10W,10K OHM	20.00		R3,4,7,8,11,12,15,16
				R19,20,23,24,27,28
				R31,32,35,36,39,40
202-09899	RESSM,RO,5%,1/10W,47 OHM	3.00		R412,416,420
202-10426	RESSM,RO,5%,1/10W,15K OHM	4.00		R542-545
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	8.00		R559-561,566,568
				R573,576,577

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
202-10558	RESSM,RO,5%,1/10W,47K OHM	23.00		R149,150,155,156,167 R168,184,185,232,233 R256-265,413,417,421
202-10559	RESSM,RO,5%,1/10W,100 OHM	14.00		R175,176,186,187,193 R194,200,201,207,208 R214,215,221,222
202-10569	RESSM,RO,5%,1/10W,10 OHM	11.00		R166,182,190,197 R204,211,218,225 R238,245,252
202-10571	RESSM,RO,5%,1/10W,100K OHM	16.00		R43,44,51,52,59,60 R67,68,75,76,83,84 R91,92,99,100
202-10585	RESSM,RO,5%,1/4W,51 OHM	12.00		R288,291,294,297,300 R303,306,309,312,315 R318,321
202-10586	RESSM,RO,5%,1/4W,100 OHM	36.00		R1,2,5,6,9,10,13,14 R17,18,21,22,25,26 R29,30,33,34,37,38 R41,42,49,50,57,58 R65,66,73,74,81,82 R89,90,97,98
202-10598	RESSM,RO,5%,1/10W,330 OHM	1.00	03/28/01■	R579
202-10890	RESSM,RO,5%,1/10W,220 OHM	1.00		R578
202-10948	RESSM,RO,5%,1/10W,390 OHM	1.00		R183
202-11041	RESSM,RO,5%,1/10W,680 OHM	2.00		R165,181
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	6.00		R239,240,246,247 R253,254
203-11743	RESSM,RO,1%,1/10W,100K OHM	36.00		R422-424,432-434 R442-444,452-454 R462-464,472-474 R482-484,492-494 R502-504,512-514 R522-524,532-534
203-11980	RESSM,THIN,1%,1/10W,10.0K OHM	36.00		R121,122,125,126,129 R130,133,134,137,138 R141,142,425,428,435 R438,445,448,455,458 R465,468,475,478,485 R488,495,498,505,508 R515,518,525,528,535 R538
203-12371	RESSM,THIN,1%,1/10W,2.74K OHM	36.00		R274,277,282,283,342 R345,350,351,356,359 R364,365,370,373,378 R379,384,387,392,393 R398,401,406,407,431 R441,451,461,471,481 R491,501,511,521 R531,541
203-12372	RESSM,THIN,1%,1/10W,4.99K OHM	68.00		R105-120,145,146 R151,152,278-280,285 R346-348,353,360,361 R363,366,374,375,377 R380,388,389,391,394 R402,403,405,408,427 R430,437,440,447,450 R457,460,467,470,477 R480,487,490,497,500

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
				R507,510,517,520,527
				R530,537,540
203-12719	RESSM,THIN,1%,1/10W,2.00K OHM	14.00		R228,229,286,287,295
				R296,298,299,307,308
				R310,311,319,320
203-12969	RESSM,THIN,1%,1/10W,316 OHM	8.00		R171,174,268,271,322
				R325,331,334
203-12970	RESSM,THIN,1%,1/10W,590 OHM	48.00		R45-48,53-56,61-64
				R69-72,77-80,85-88
				R93-96,101-104,169
				R172,266,269,272,275
				R340,343,354,357,368
				R371,382,385,396,399
203-13132	RESSM,THIN,1%,1/10W,3.01K OHM	24.00		R123,124,127,128,131
				R132,135,136,139,140
				R143,144,147,148
				R153,154,170,173
				R267,270,323,324
				R332,333
203-13134	RESSM,THIN,1%,1/10W,1.00K OHM	24.00		R273,276,281,284,341
				R344,349,352,355,358
				R362,367,369,372,376
				R381,383,386,390,395
				R397,400,404,409
203-13537	RESSM,THIN,1%,1/10W,5.62K OHM	6.00		R289,292,301,304
				R313,316
203-13638	RESSM,THIN,1%,1/10W,2.49K OHM	16.00		R230,231,290,293,302
				R305,314,317,327-330
				R336-339
203-14296	RESSM,THIN,1%,1/10W,6.49K OHM	24.00		R426,429,436,439,446
				R449,456,459,466,469
				R476,479,486,489,496
				R499,506,509,516,519
				R526,529,536,539
204-14794	RES,WW,1%,5W,10 OHM,FP	1.00		R255
240-09367	CAPSM,ELEC,10UF,25V,NONPOL,20%	20.00		C43,44,47,48,51,52
				C55,56,59,60,63,64
				C67,68,71,72,494-497
240-09786	CAP,ELEC,100UF,25V,RAD,LOW ESR	4.00		C329,330,333,336
240-11111	CAPSM,ELEC,47UF,6V,NONPOL,20%	22.00		C95,96,99,100,151
				C152,183,186,189,192
				C195,198,241,244,251
				C254,261,264,271,274
				C281,284
240-12330	CAPSM,ELEC,2.2UF,35V,20%	12.00		C347,359,371,383,395
				C407,419,434,446,458
				C470,482
240-13217	CAPSM,ELEC,47UF,16V,20%	6.00		C157,158,167,168
				C177,178
240-13642	CAP,ELEC,47UF,25V,RAD,NPOL,6D	20.00		C3,4,7,8,11,12,15,16
				C19,20,23,24,27,28
				C31,32,35,36,39,40
241-09798	CAPSM,TANT,10UF,10V,20%	26.00		C101,104,107,110,113
				C116,119,122,125,128
				C131,134,137,140,143
				C146,153,156,159,163
				C166,169,173,176
				C179,431
241-11799	CAPSM,TANT,4.7UF,6.3V,20%	79.00		C106,112,117,123,129
				C135,141,147,161,171
				C181,221,224,225,228

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
				C233,236,237,240,292 C295,299,302,304,307 C311,314,316,319,323 C326,350,352,355,357 C362,364,367,369,374 C376,379,381,386,388 C391,393,398,400,403 C405,410,412,415,417 C422,424,427,429,437 C439,442,444,449,451 C454,456,461,463,466 C468,473,475,478,480 C485,487,490,492
244-10423	CAP,MYL,.22UF,50V,RAD,5%,BOX	8.00		C327,331,334,337,340 C342,344,346
244-10592	CAP,MYL,2200PF,100V,RAD,5%	26.00		C184,185,190,191,196 C197,217,218,229,230 C242,243,252,253,262 C263,272,273,282,283 C291,297,303,309 C315,321
245-09291	CAPSM,CER,470PF,50V,COG,5%	32.00		C187,188,193,194,199 C200,202,203,219,220 C231,232,245,246,249 C250,255,256,259,260 C265,266,269,270,275 C276,279,280,285,286 C289,290
245-10416	CAPSM,CER,1000PF,50V,COG,5%	12.00		C201,204,247,248 C257,258,267,268 C277,278,287,288
245-10544	CAPSM,CER,220PF,50V,COG,5%	12.00		C351,363,375,387 C399,411,423,438 C450,462,474,486
245-10561	CAPSM,CER,100PF,50V,COG,5%	12.00		C205-216
245-10562	CAPSM,CER,150PF,50V,COG,10%	68.00		C1,2,5,6,9,10,13,14 C17,18,21,22,25,26 C29,30,33,34,37,38 C41,42,45,46,49,50 C53,54,57,58,61,62 C65,66,69,70,328,332 C335,338,339,341,343 C345,348,349,360,361 C372,373,384,385,396 C397,408,409,420,421 C435,436,447,448,459 C460,471,472,483,484
245-10587	CAPSM,CER,18PF,50V,COG,10%	26.00		C73-94,97,98,149,150
245-12485	CAPSM,CER,.1UF,25V,Z5U,20%	262.00		+/-BC1-27 +BC29A,B;-BC29 +BC31A,B;-BC31 +/-BC38,42 +BC43-47A,B;-BC43-47 +/-BC48-55,58-62 BC63,65 +/-BC68-74 BC75,76,85,86 +/-BC87-91

PART NO	DESCRIPTION	QTY	EFFECTIVE■	INACTIVE	REFERENCE
					BC92
					+BC93A,B;-BC93
					BC94;BC95A-H
					BC101,102
					C102,103,105,108,109
					C111,114,115,118,120
					C121,124,126,127,130
					C132,133,136,138,139
					C142,144,145,148,154
					C155,160,162,164,165
					C170,172,174,175,180
					C182,222,223,226,227
					C234,235,238,239,293
					C294,296,298,300,301
					C305,306,308,310,312
					C313,317,318,320,322
					C324,325,353,354,356
					C358,365,366,368,370
					C377,378,380,382,389
					C390,392,394,401,402
					C404,406,413,414,416
					C418,425,426,428,430
					C432,433,440,441,443
					C445,452,453,455,457
					C464,465,467,469,476
					C477,479,481,488,489
					C491,493
270-00779	FERRITE,BEAD	20.00			FB1-20
270-06671	FERRITE CHOKE,2.5 TURN	4.00			FB26-29
270-09799	FERRITESM,CHIP,600 OHM,1206	29.00			FB21-25,30,33,36,39
					FB42,45,48,51-58
					FB61,64,67,70,73-77
270-11545	FERRITESM,CHIP,600 OHM,0805	24.00			FB31,32,34,35,37,38
					FB40,41,43,44,46,47
					FB49,50,59,60,62,63
					FB65,66,68,69,71,72
300-01030	DIODE,1N4004 AND 4005	1.00		■06/01/01	D26
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	16.00			D1-16
300-11599	DIODESM,GP,1N4002,MELF	5.00		■06/01/01	D17-21
300-11599	DIODESM,GP,1N4002,MELF	6.00	06/01/01■		D17-21,26
300-14286	DIODESM,SCHOTTKY,1A,SMB	2.00			D24,25
310-10510	TRANSISTORSM,2N3904,SOT23	13.00			Q4,6,8,10,12,14,16
					Q18,20,22,24,26,28
310-10565	TRANSISTORSM,2N3906,SOT23	12.00			Q5,7,9,11,13,15,17
					Q19,21,23,25,27
310-10566	TRANSISTORSM,2N4401,SOT23	3.00			Q1-3
330-10522	ICSM,DIGITAL,74HC04,SOIC	2.00			U65,94
330-10536	ICSM,DIGITAL,74HC273,SOIC	7.00			U63,75,76,85,86
					U92,101
340-00742	IC,LINEAR,7805 (LM 340 T-5)	1.00			U77
340-10550	ICSM,LIN,CS3310,VOL CTL,SOIC	11.00			U28,30,32-37,39-41
340-10552	ICSM,LIN,MC33078,DU OPAMP,SOIC	19.00			U10,12,19,20,38,42
					U48-55,58-62
340-11597	ICSM,LIN,TL072,DUAL OPAMP,SOIC	9.00			U1-8,21
340-12367	ICSM,LIN,OP275,DU OP AMP,SOIC	8.00			U9,11,13-18
340-12936	ICSM,LIN,OPA2134,DU OP AMP,SO8	12.00			U68-74,87-91
346-10549	ICSM,SS SWITCH,DG408,SOIC	6.00			U22-27
346-14451	ICSM,SS SW,DG411QUAD,1P1T,SOIC	8.00		■08/29/01	U29,31,43-47,93
346-14583	ICSM,SS SW,ADG451QUAD,1P1T,SOI	8.00	08/29/01■		U29,31,43-47,93
350-13855	ICSM,FPGA,XCS10-3,14X14,TQFP	1.00			U95
355-13829	ICSM,ADC,AKM5383,24B,96KHZ,SOP	3.00			U64,66,67

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
355-13987	ICSM,DAC,AD1853,24BIT,SSOP	12.00		U78-84,96-100
355-14761	ICSM,DAC,AK4395,24BIT,VSOP	2.00		U56,57
410-11639	RELAY,2P2T,DIP,5V,HI SENS	10.00		RY1-10
430-10419	LEDSM,INNER LENS,RED	1.00	03/28/01■	D23
430-10421	LEDSM,INNER LENS,GRN	1.00		D22
510-03961	CONN,POST,100X025,HDR,2MCG	1.00		W1
510-13149	CONN,RCA,PCRA,1FCGX2V,WH/RED,G	18.00		J1-18
510-13877	CONN,POST,.100,HDR,2X5MCG,LP	1.00		J30
510-13941	CONN,POST,.100,HDR,2X17MCG,LP	1.00		J33
510-14079	CONN,POST,156X045,HDR,4MC,LOK	1.00		J25
510-14080	CONN,POST,156X045,HDR,6MC,LOK	1.00		J26
520-00941	IC SCKT,8 PIN,LO-PRO	1.00		U102
640-01701	SCRW,4-40X1/4,PNH,PH,ZN	1.00		U77 (H/S)
641-13116	SCRW,TAP,AB,4X3/8,FH,PH,BZ	18.00		J1-18 (RCAS TO BRKT)
680-12320	CABLE,100,PLUG/SCKT,2X30C,1.5"	1.00		J32 (ANLG TO MN BD)
701-14088	BRACKET,ANALOG BD,MC12	1.00		
704-14452	HEATSINK,TO220,MTTAB,NUT,1.45H	1.00		U77

MC-12/MC-12 Balanced SWITCH/LED BOARD

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	8.00		R39-46
202-10597	RESSM,RO,5%,1/10W,180 OHM	15.00		R1-12,47-49
202-10599	RESSM,RO,5%,1/10W,3K OHM	2.00		R37,38
202-10945	RESSM,RO,5%,1/10W,1.5K OHM	13.00		R13-24,50
202-10948	RESSM,RO,5%,1/10W,390 OHM	12.00		R25-36
240-09786	CAP,ELEC,100UF,25V,RAD,LOW ESR	1.00		C10
245-12485	CAPSM,CER,.1UF,25V,Z5U,20%	9.00		C1-9
300-10509	DIODESM,1N914,SOT23	6.00		D37,38,43-46
310-10510	TRANSISTORSM,2N3904,SOT23	1.00		Q1
330-10372	ICSM,DIGITAL,74HC574,SOIC	7.00		U1-7
330-10537	ICSM,DIGITAL,74HC541,SOIC	1.00		U8
330-14244	ICSM,DIGITAL,74VHCT138,SOIC	1.00		U9
430-13639	LEDSM,BLU,30MCB,AX,ZBEND,2.5MM	12.00		D25-36
430-13888	LEDSM,RED,60MCD,AX,ZBEND,2.5MM	15.00		D1-12,39-41
430-14527	LEDSM,SYEL,250MCD,AX,ZBEND,2.5	13.00		D13-24,42
453-13899	SWSM,PBM,1P1T,6.2MMSQ,200GF	42.00		SW1-42
510-13145	CONN,POST,.100,HDR,2X7MCG,LP	2.00		J1,2
680-14083	CABLE,100,PLUG/SCKT,2X13C,2"L	1.00		SW/LED TO MAIN BD

MC-12/MC-12 Balanced IR/ENCODER BOARD

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
202-00528	RES,CF,5%,1/4W,820 OHM	1.00		R1
202-00530	RES,CF,5%,1/4W,1.2K OHM	1.00		R2
202-00531	RES,CF,5%,1/4W,1.5K OHM	1.00		R3
245-03609	CAP,CER,.1UF,50V,Z5U,AX,80/20%	2.00		C1,2
345-14780	IC,INTER,GP1U28,38KHZ,IR DET	1.00		U1B
430-10594	LED,T1-3/4,IR	1.00		D1
430-14487	LED,T1,BLU,430NM	1.00		SYSTEM ON D4
430-14787	LED,T1,RED,700NM	1.00		OVERLOAD D2
430-14788	LED,T1,YEL,585NM	1.00		IR ACK D3
452-13640	SW,RTY,ENC,24POS,INC B,25L,VRT	1.00		SW1
630-14778	SPCR,LED,T1,.375"H	3.00		D2-4
680-14082	CABLE,100,PLUG/SCKT,2X7C,3"L	1.00		IR/ENC BD (J1) TO SW/LED BD

MC-12/MC-12 Balanced STANDBY BOARD

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
430-13888	LEDSM,RED,60MCD,AX,ZBEND,2.5MM	1.00		D1
453-13899	SWSM,PBM,1P1T,6.2MMSQ,200GF	1.00		SW1
510-10546	CONN,POST,079,HDR,4MC	1.00		J1

MC-12/MC-12 Balanced MEMORY BOARD

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
202-09873	RESSM,RO,5%,1/10W,10K OHM	1.00		R1
245-12485	CAPSM,CER,.1UF,25V,Z5U,20%	3.00		C5; C1,2 (IF U1 POP); C3,4 (IF U2 POP)
350-14466	ICSM,FLASH,16M,MC12,V1.01	1.00		U1 (TSOP PKG) OR
PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
				U2 (SOIC PKG)
350-14786	IC,ROM,27C020,MC12,MEM,V1.00	1.00		U3
500-13644	CONN,EURO,C,48P,ABC,PLUG,RA	1.00		J1
520-04999	IC SCKT,32 PIN,MACH,TIN	1.00		U3

MC-12/MC-12 Balanced VCO ASSEMBLY

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
202-09899	RESSM,RO,5%,1/10W,47 OHM	1.00		R1
245-09895	CAPSM,CER,10PF,50V,COG,10%	1.00		C3
245-12485	CAPSM,CER,.1UF,25V,Z5U,20%	4.00		C1,2,4,5
270-11545	FERRITESM,CHIP,600 OHM,0805	1.00		FB1
270-14359	COILSM,VAR,1UH,5%,5.6X6.2X6MM	1.00		L1
300-13881	DIODESM,VARACTOR,BB132	1.00		D1
340-14528	ICSM,LIN,MC100EL1648,VCO,SOIC	1.00		U1
510-14836	CONN,POST,100X025,HDR,5MC,RA	1.00		J1
700-14838	HOUSING,VCO,MC12	1.00		
700-14839	COVER,VCO,MC12	1.00		

MC12 Balanced ONLY

MC-12B XLR BOARD

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
202-10943	RESSM,RO,5%,1/10W,22K OHM	28.00		R3-30
202-10948	RESSM,RO,5%,1/10W,390 OHM	2.00		R1,2
203-12720	RESSM,THIN,1%,1/10W,2.94K OHM	14.00		R33,38,41,46,49,54 R57,62,65,70,73,78 R81,86
203-13132	RESSM,THIN,1%,1/10W,3.01K OHM	14.00		R31,36,39,44,47,52 R55,60,63,68,71,76 R79,84
203-14874	RESSM,THIN,1%,1/10W,6.04K OHM	4.00		R32,34,35,37
203-14891	RESSM,THIN,1%,1/10W,9.09K OHM	24.00		R40,42,43,45,48,50 R51,53,56,58,59,61 R64,66,67,69,72,74 R75,77,80,82,83,85
240-13642	CAP,ELEC,47UF,25V,RAD,NPOL,6D	28.00		C43,44,49,50,53,54 C59,60,63,64,69,70 C73,74,79,80,83,84 C89,90,93,94,99,100 C103,104,109,110
240-13803	CAP,ELEC,560UF,35V,RAD,LOW ESR	2.00		C156,157
241-14676	CAPSM,TANT,1UF,25V,20%	28.00		C45,46,51,52,55,56 C61,62,65,66,71,72 C75,76,81,82,85,86

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
				C91,92,95,96,101,102
				C105,106,111,112
245-10562	CAPSM,CER,150PF,50V,COG,10%	28.00		C1,3,4,6,7,9,10,12
				C13,15,16,18,19,21
				C22,24,25,27,28,30
				C31,33,34,36,37,39
				C40,42
245-10587	CAPSM,CER,18PF,50V,COG,10%	24.00		C119,120,123-126
				C129-132,135,136
				C138,139,142-145
				C148-151,154,155
245-10588	CAPSM,CER,33PF,50V,COG,10%	4.00		C113,114,117,118
245-12485	CAPSM,CER,.1UF,25V,Z5U,20%	14.00		C115,116,121,122
				C127,128,133,134
				C140,141,146,147
				C152,153
270-00779	FERRITE,BEAD	28.00		FB1-28
270-06671	FERRITE CHOKE,2.5 TURN	2.00		FB29,30
300-11599	DIODESM,GP,1N4002,MELF	2.00		D1,2
310-10566	TRANSISTORSM,2N4401,SOT23	2.00		Q1,2
340-10552	ICSM,LIN,MC33078,DU OPAMP,SOIC	7.00		U15-21
340-13911	ICSM,LIN,DRV134,BAL LINE DRVR	14.00		U1-14
410-11639	RELAY,2P2T,DIP,5V,HI SENS	14.00		RY1-14
510-10881	CONN,XLR,3MC,PCRA,PLASTIC CMPT	14.00		J1-14
510-14890	CONN,POST,.100,HDR,2X17MCG,LK	1.00		J15
620-12428	LUG,#4,INT STAR,XLR GND	14.00		J1-14

MC-12/MC-12 Balanced CHASSIS ASSEMBLY

*Note: * items are on MC12 only; ^ items are on MC12B only.*

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
120-09621	ADHESIVE,THRD LOCK,LOCTITE#242	0.00		DSUB JSCKT
490-13872	CONN,PLUG,.200,6FC,RA,12-30G	1.00		REAR PANEL
527-12974	CONN,DSUB,JSCKT,4-40,.187X.25	4.00		DCONN TO R.PANEL
540-02472^	PLUG,HOLE,3/8",BLK	4.00		
541-13631*	FOOT,2.0X.5H,ALUM,BLK	4.00		CHASSIS
630-15011	SPCR,#6CLX3/16,1/4RD,NYL	2.00		ANLG SHLD TO ANLG BD
635-13637	SPCR,M3X34MM,M/F,6MM HEX	3.00		ANLG BD TO MAIN BD
635-14779	SPCR,M3X14MM,6MM HEX	1.00		MEM BD TO CHASSIS
640-02377	SCRW,4-40X1/4,PNH,PH,BLK	3.00		OPTO TO MAIN BD(2);
				MAIN BD TO R.PNL(1)
640-10467	SCRW,M3X6MM,FH,PH,BZ	3.00		PS SPT TO CHAS(2);
				MEM BD TO CHAS(1)
640-10495	SCRW,M3X12MM,PNH,PH,ZN	2.00		ANLG SHLD TO ANLG BD
640-10496	SCRW,4X10MM,PNH,PH,ZN	2.00		F.PANEL TO CHAS
640-10496*	SCRW,4X10MM,PNH,PH,ZN	4.00		FEET TO CHAS
640-10496^	SCRW,4X10MM,PNH,PH,ZN	7.00		12B FP TO 1U CHAS(3);
				1U CHAS TO 3U CHAS(4)
640-10498	SCRW,M3X6MM,PNH,PH,BZ	29.00		PS SPT TO CHAS(3);
				MAIN BD TO CHAS(7);
				F.PANEL TO CHAS(3);
				OPT PNL TO REAR(2);
				ANLG BD TO R.PNL(5);
				ANLG ASSY TO MNBD(3);
				VIDEO BDS TO R.PNL(5);
				MEM BD TO CHAS(1)
640-10498^	SCRW,M3X6MM,PNH,PH,BZ	2.00		XLR BD TO 1U CHASSIS
640-13645	SCRW,M4X10MM,FH,SCKT,BZ	12.00		COVER TO CHASSIS
641-01703*	SCRW,TAP,AB,4X1/4,PNH,PH,ZN	2.00		ACCESS PANEL TO CHAS

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
641-10989	SCRW,TAP,AB,4X3/8,PNH,PH,BZ	6.00		R.PANEL TO CHASSIS
641-11466	SCRW,TAP,#4X3/8,PNH,PH,BZ,TRI	5.00		OPTO CONN TO R.PNL(1); RCA CONN TO R.PNL(4)
641-14672	SCRW,TAP,M2.5X8MM,PNH,PH,BZ,TR	2.00		XLR CONN TO R.PNL
641-14776^	SCRW,TAP,#4X3/8,FH,PH,ZN,TRI	28.00		XLR BD TO 1U CHASSIS
643-10491	NUT,M3X.5MM,KEP,ZN	2.00		ANLG SHLD TO ANLG BD
680-14494^	CABLE,.10,SCKTX2-180,2X17C,6"	1.00		XLR BD (J15) TO ANLG BD (J33)
680-14539	CABLE,HSG/HSG,4C,4"	1.00		ANLG BD (J25) TO VIDEO BD (J22)
700-14084	CHASSIS,3U,MC12	1.00		
700-14085	COVER,3U,MC12	1.00		
700-14677^	CHASSIS,1U,MC12B	1.00		
701-15010	SHIELD,ANLG BD,MC-12/MC-12 Balanced	1.00		
702-14094	PANEL,REAR,MC12	1.00		
702-14097	PANEL,OPTION,BLANK,MC12	1.00		REAR PANEL
702-14454^	PANEL,FRONT,1U,MC12B	1.00		
702-14495*	PANEL,ACCESS,MC12	1.00		CHASSIS BOTTOM
720-13632	PAD,FOOT,1.438DIA	4.00		MC12: 3U CHAS BTM MC12B: 1U CHAS BTM
720-14749	TAPE,FOAM,SGL-STK,1/4THX1"W	3.00		
740-09538	LABEL,S/N,CHASSIS,PRINTED	1.00		REAR PANEL
740-14888	LABEL,DOLBY/THX/EX/DTS-ES/WARN	1.00		CHASSIS BOTTOM

MC-12/MC-12 Balanced POWER SUPPLY ASSEMBLY

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
454-13850	SW,ROCKER,2P1T,5A/80A@250,TV5	1.00		
490-11462	CONN,AC,3MC,SNAP,04TH,IEC,10A	1.00		
530-02488	TIE,CABLE,NYL,.14"X5 5/8"	2.00		FERRITE SLEEVE TO PS SUPPORT
640-10467	SCRW,M3X6MM,FH,PH,BZ	2.00		PWR SW TO PS SPT
640-12534	SCRW,M3X20MM,PNH,PH,BZ	4.00		FAN TO PS SPT
640-13622	SCRW,6-32X1/4,HWH,SL,ZN	2.00		PS TO PS SPT
643-10492	NUT,M4X.7MM,KEP,ZN	1.00		CHASSIS GND
644-01740	WSHR,LOCK,SPLIT,#6	2.00		PS TO PS SPT
644-10494	WSHR,FL,M4CLX9ODX.8MM THK	1.00		CHASSIS GND
680-11461	WIRE,18G,G/Y,2.5",187QDC/LUG#8	1.00		AC CONN TO CHAS GND
680-14536	CABLE,PWR,.187/.110QDC,SLV,4.5	1.00		AC CONN TO PWR SW
680-14537	CABLE,PWR,HSG/.110QDC,2C,5"	1.00		PWR SW TO PWR SUP
680-14538	CABLE,HSG/HSG,10C,SLV,16/13"	1.00		PWR SUP TO MAIN(J31) AND ANLG(J26) BDS
700-14086	SUPPORT,PS,MC12	1.00		
720-14852	GASKET,FAN,1.5D/1.7SQ,BLK	1.00		FAN TO PS SPT
740-08556	LABEL,GROUND SYMBOL,0.5"DIA	1.00		PS SUPPORT
740-14798	LABEL,FUSE,CAUTION,F1,4A/250V	1.00		PS SUPPORT
750-14532	PWR SUP,+-5V/+-15V,90W	1.00		

MC-12/MC-12 Balanced FAN ASSEMBLY

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
410-14851	FAN,40X40X10MM,12VDC,3.43CFM	1.00		
525-12536	CONN,CONT,CRIMP,22-26AWG,AMP	2.00		
527-12537	CONN,HSG,CRIMP,.100X2,POL,LK	1.00		

MC-12/MC-12 Balanced FRONT PANEL MECHANICAL ASSEMBLY

PART NO	DESCRIPTION	QTY	EFFECTIVE■INACTIVE	REFERENCE
430-13143	DISPLAY,VF,20X2 CHAR,5X8DOT	1.00		
550-13633	BUTTON,.276X.572,BLK	2.00		
550-13634	BUTTON,.276X.572,BLK,W/LTPIPE	41.00		
550-14090	KNOB,2.00X.95H,6MM,ALUM,PEWTER	1.00		ENCODER

PART NO	DESCRIPTION	QTY	EFFECTIVE▪INACTIVE	REFERENCE
635-14526	SPCR,M3CLX6MM,6MMRD	1.00		IR/ENC BD
640-01841	SCRW,2-56X1/4,PNH,PH,ZN	4.00		DISPLAY TO FP
640-10495	SCRW,M3X12MM,PNH,PH,ZN	1.00		IR/ENC BD
640-10496	SCRW,4X10MM,PNH,PH,ZN	2.00		SPT BRKT TO FP
640-10498	SCRW,M3X6MM,PNH,PH,BZ	22.00		OPT BD BRKT(2); SHIELD TO FP(10); SW/LED BD TO FP(8); STANDBY BD TO FP(2)
680-14693	CABLE,100,PLUG/SCKT,2X7C,11.5"	1.00		DSPLY TO SW/LED BD.
680-14854	CABLE,079,SCKT/SCKT,4C,4",CMP	1.00		STANDBY TO MAIN BD
701-13630	BRACKET,SUPPORT,COVER,MC12	1.00		
701-14496	BRACKET,OPT BD,MC12	1.00		
701-14858	SHIELD,6.7X1.8X.4"H	1.00		
702-14091	PANEL,FRONT,MC12	1.00		
703-14098	LENS,6.36X1.55,MC12	1.00		

MC-12/MC-12 Balanced VIDEO MECHANICAL ASSEMBLY

PART NO	DESCRIPTION	QTY	EFFECTIVE▪INACTIVE	REFERENCE
640-10498	SCRW,M3X6MM,PNH,PH,BZ	6.00		VIDEO BD TO BRKT
641-13116	SCRW,TAP,AB,4X3/8,FH,PH,BZ	18.00		VIDEO BD TO BRKT
643-04942	NUT,1/2-28,HEX,SMALL,BRASS/NI	6.00		BNC TO VIDEO BRKT
644-04943	WSHR,INT STAR,1/2CLX5/8ODX.022	6.00		BNC TO VIDEO BRKT
701-14087	BRACKET,VIDEO BD,MC12	1.00		

MC-12/MC-12 Balanced PACKAGING/MISCELLANOUS

PART NO	DESCRIPTION	QTY	EFFECTIVE▪INACTIVE	REFERENCE
070-14710	NOTES,ERRATA,MC12/B	1.00		
070-14773	GUIDE,USER,MC12/B	1.00		
460-08345	BAT,ALK,AA	2.00		
730-14767	BOX,21-3/4X19X12,LEXICON	1.00		INNER BOX
730-14769	BOX,22-1/2X19-3/4X13-1/4,BLANK	1.00		OUTER BOX
730-14770	INSERT,CORR/FOAM,ACCESS,MC12/B	1.00		
730-14771	INSERT,FOAM,BASE,3&4UX15	1.00		
730-14772	INSERT,FOAM,TOP,3&4UX15	2.00		
750-14521	REMOTE CONTROL,MC12	1.00		

MC-12/MC-12 Balanced POWER CORD OPTIONS

PART NO	DESCRIPTION	QTY	EFFECTIVE▪INACTIVE	REFERENCE
680-09149	CORD,POWER,IEC,10A,2M,NA,SVT	1.00		N.AMER.
680-08830	CORD,POWER,IEC,6A,2M,EURO	1.00		
680-10093	CORD,POWER,IEC,5A,2M,UK	1.00		
680-10096	CORD,POWER,IEC,6A,2M,AUSTRALIA	1.00		
680-10097	CORD,POWER,IEC,6A,2M,JAPAN	1.00		
680-10094	CORD,POWER,IEC,6A,2M,ITALY	1.00		
680-10095	CORD,POWER,IEC,6A,2M,SWISS	1.00		

MC-12/MC-12 Balanced MOUNTING OPTION

PART NO	DESCRIPTION	QTY	EFFECTIVE▪INACTIVE	REFERENCE
630-08670	WSHR,FIN,#10,NYL,BLK	4.00		
640-08671	SCRW,10-32X3/4,FH,PH,BLK	4.00		
640-14680	SCRW,M4X14MM,FH,SCKT,SS	4.00		
701-13635	BRACKET,MTG,RACK,3U,MC12	2.00		

MC-12/MC-12 Balanced SPARE ASSEMBLIES

Available by special order

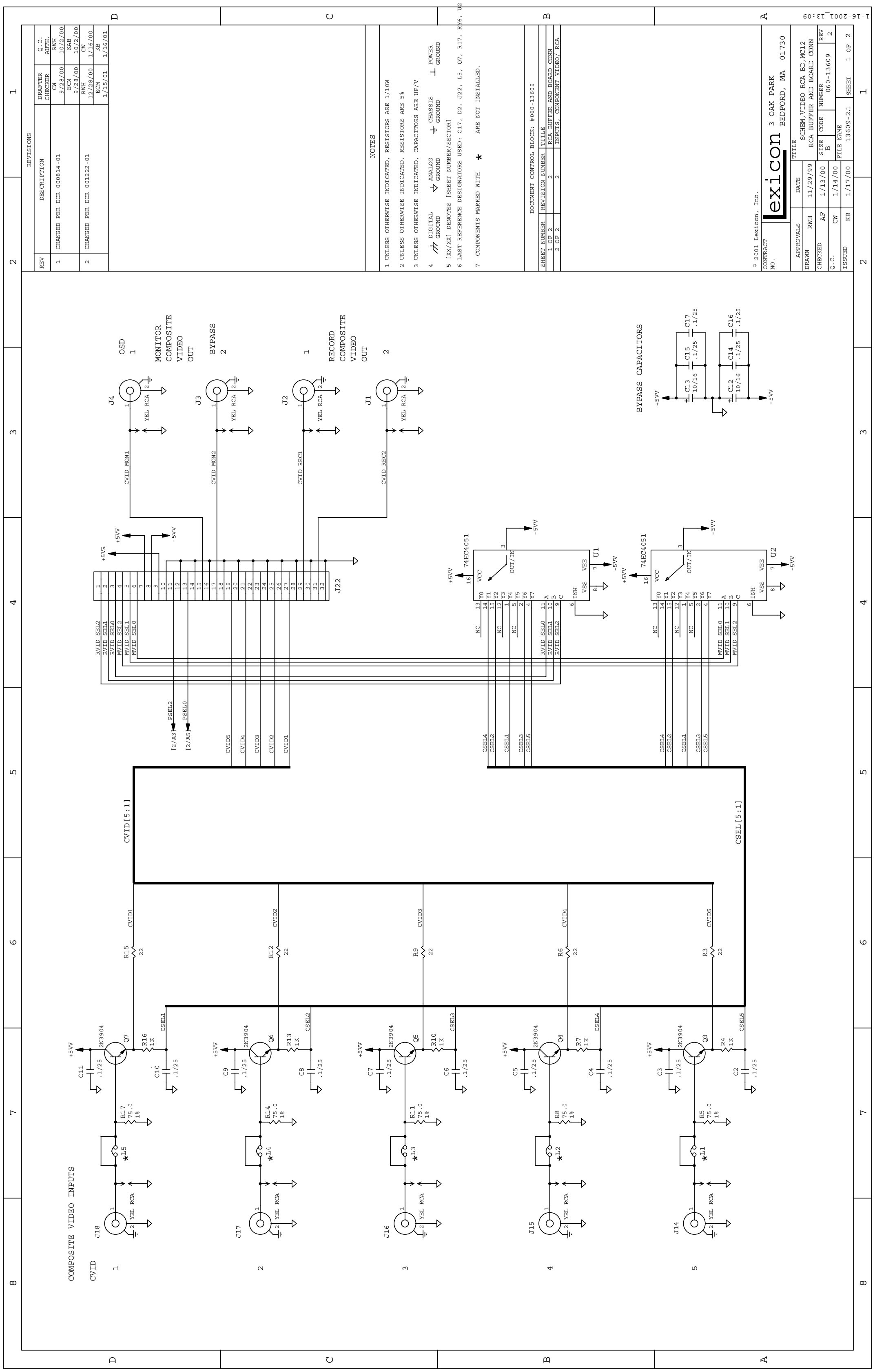
PART NO	DESCRIPTION
021-14570	PL,MAIN BD ASSY,MC12/B,TESTED
021-14571	PL,OPTO/MIC ASSY,MC12/B,TESTED
021-14572	PL,VIDEO ASSY,MC12/B,TESTED
021-14573	PL,ANLG BD ASSY,MC12/B,TESTED
021-14574	PL,SW/LED ASSY,MC12/B,TESTED
021-14575	PL,IR/ENC ASSY,MC12/B,TESTED
021-14576	PL,MEM BD ASSY,MC12/B,TESTED
021-14577	PL,XLR BD ASSY,MC12B,TESTED

Chapter 8 Schematics and Drawings

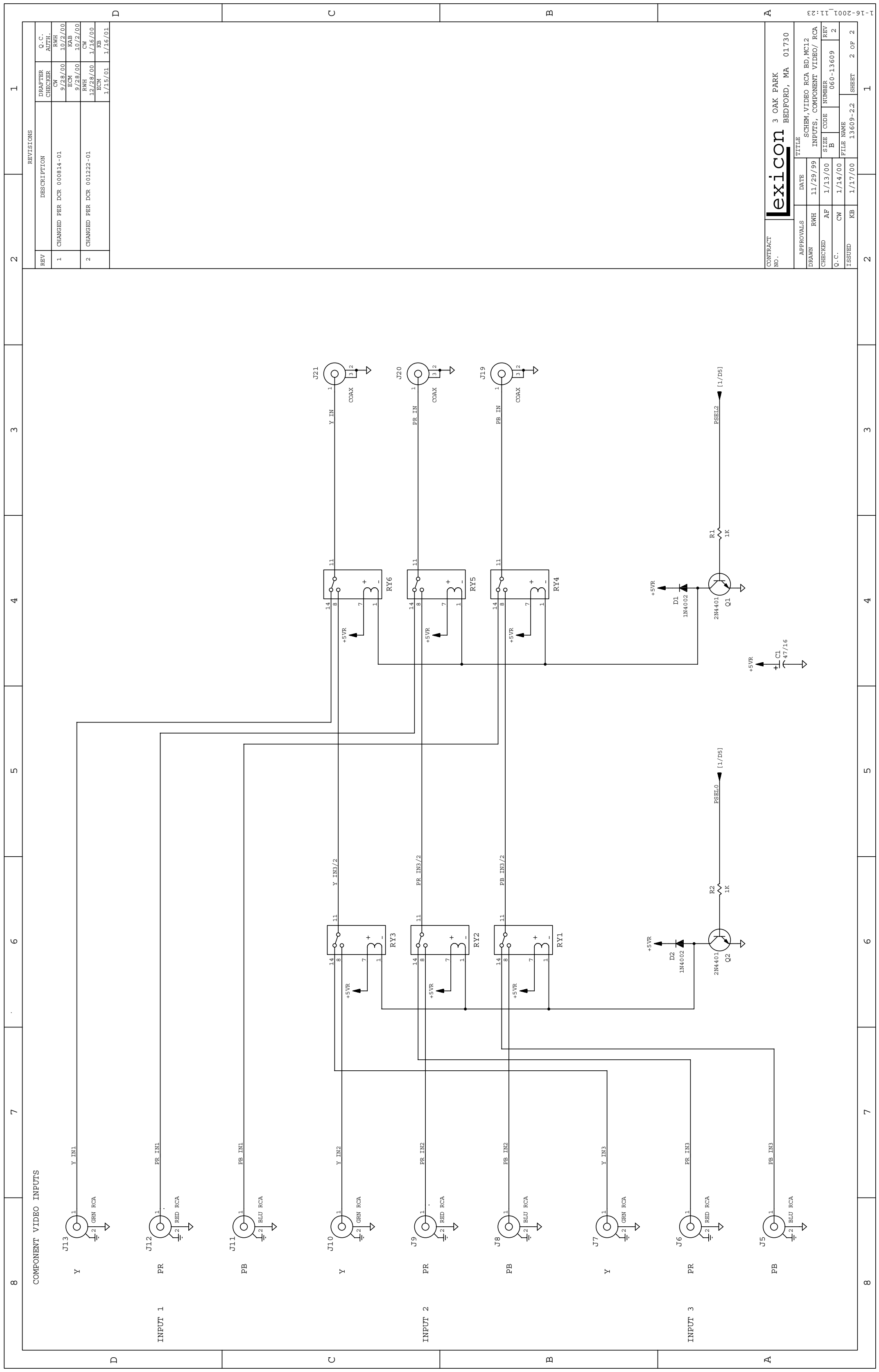
Schematics

Drawings

Your Notes:

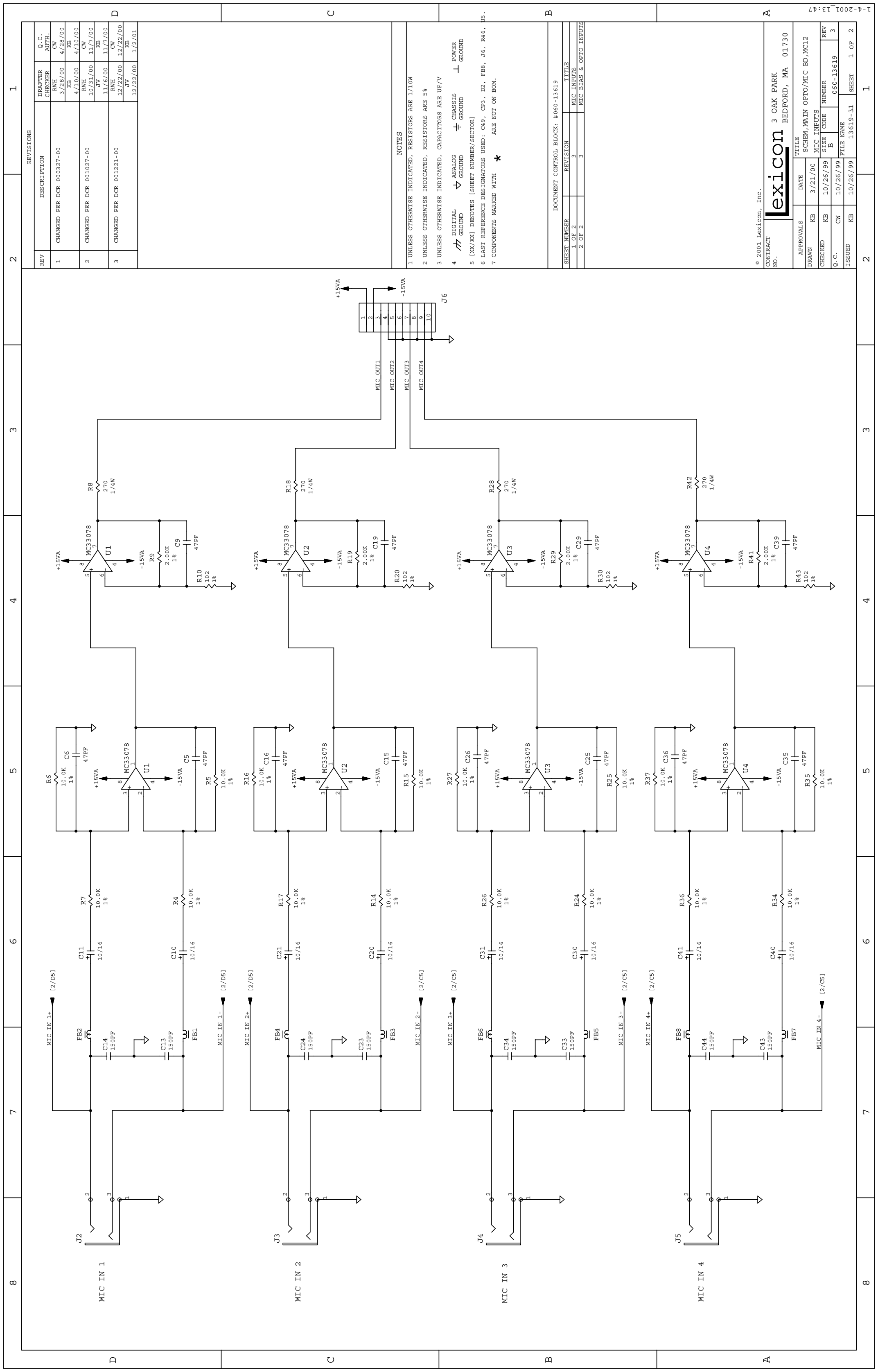

REVISIONS
1 CHANGED PER DCR 000814-01
2 CHANGED PER DCR 001222-01
NOTES
1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W
2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%
3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V
DOCUMENT CONTROL BLOCK: #060-13609
© 2001 Lexicon, Inc.
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,VIDEO RCA BD,MC12
RCA BUFFER AND BOARD CONN
060-13609
SHEET 1 OF 2
OSD
MONITOR COMPOSITE VIDEO OUT
BYPASS
RECORD COMPOSITE VIDEO OUT
BYPASS CAPACITORS
74HC4051
CVID[5:1]
CSEL[5:1]
COMPOSITE VIDEO INPUTS
CVID

Your Notes:

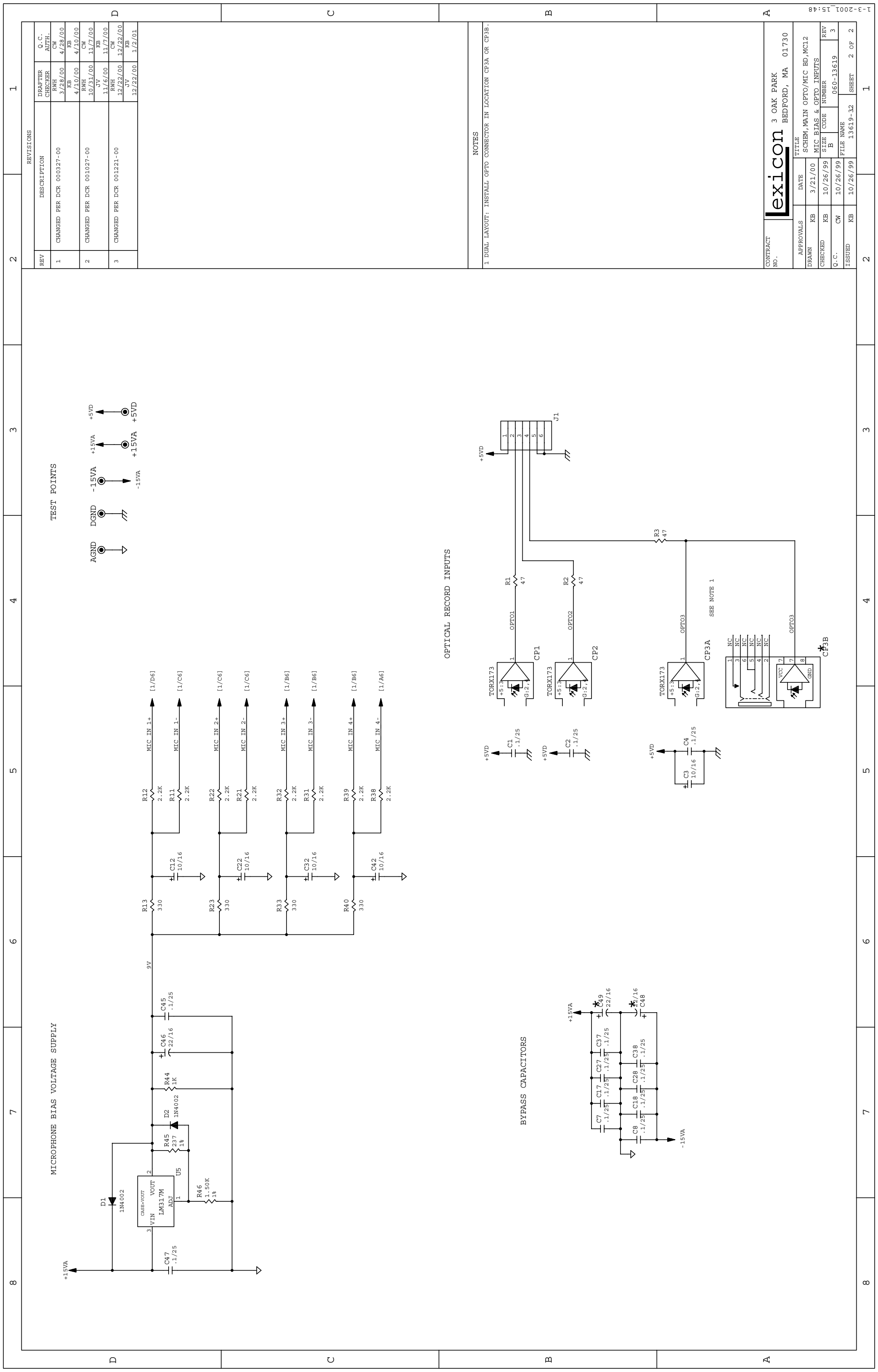


COMPONENT VIDEO INPUTS
INPUT 1
INPUT 2
INPUT 3
REVISIONS
CHANGED PER DCR 000814-01
CHANGED PER DCR 001222-01
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,VIDEO RCA BD,MC12
INPUTS, COMPONENT VIDEO/ RCA
060-13609
13609-22
2 OF 2

Your Notes:

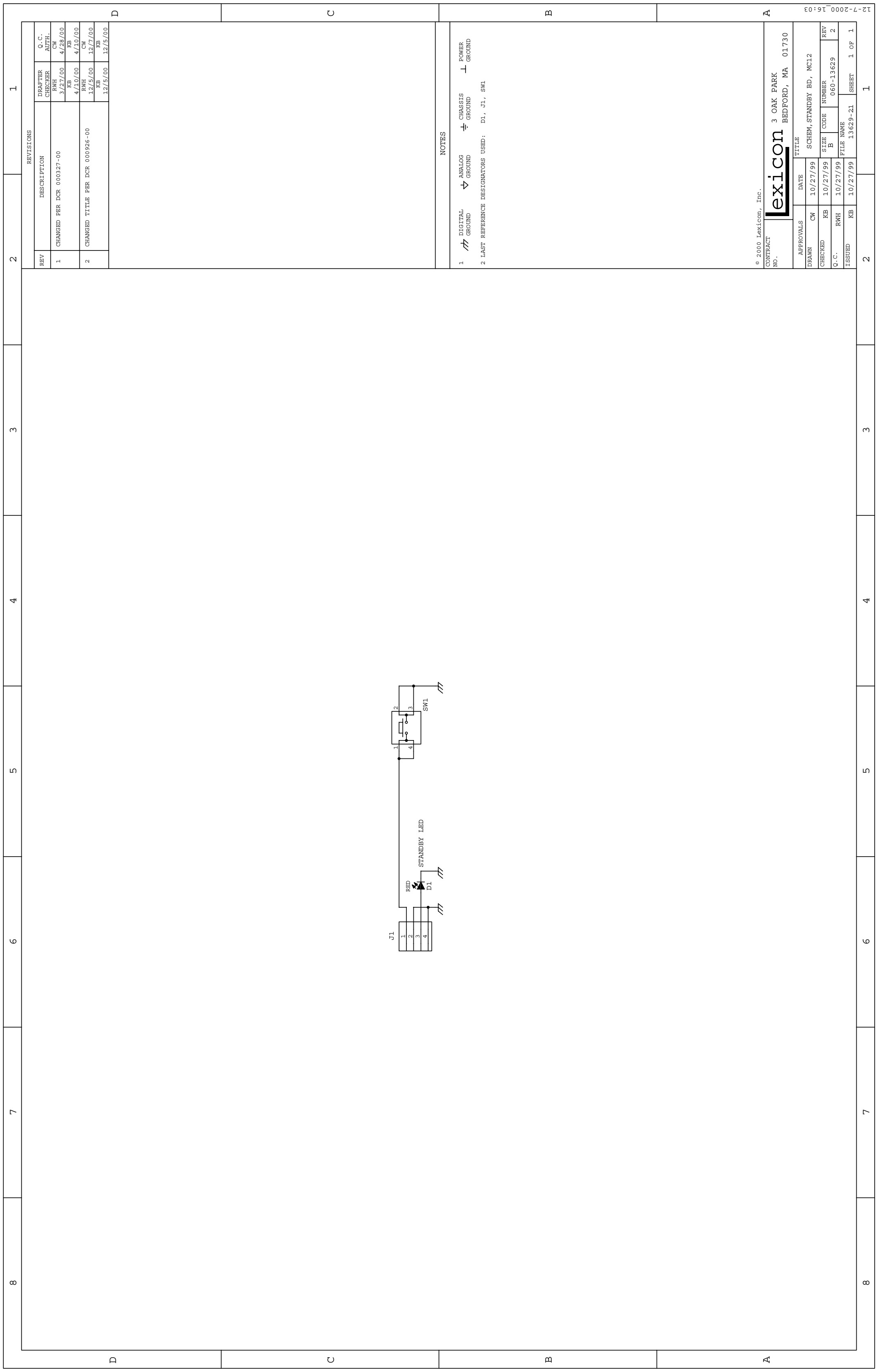

lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN OPTO/MIC BD,MC12
MIC INPUTS
060-13619
MIC IN 1
MIC IN 2
MIC IN 3
MIC IN 4

Your Notes:

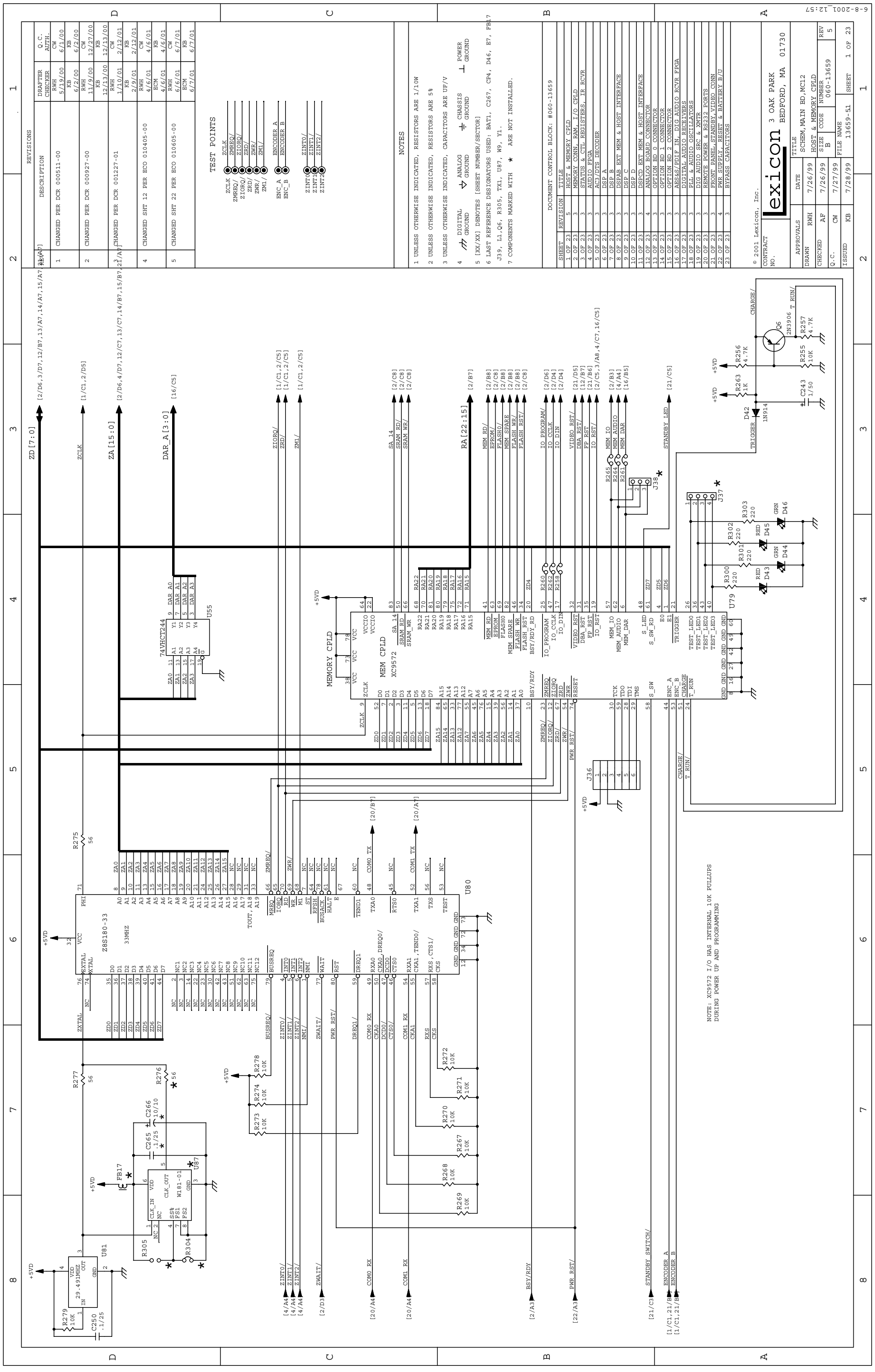


REVISIONS
REV
DESCRIPTION
1 CHANGED PER DCR 000327-00
2 CHANGED PER DCR 001027-00
3 CHANGED PER DCR 001221-00
NOTES
1 DUAL LAYOUT: INSTALL OPTO CONNECTOR IN LOCATION CP3A OR CP3B.
TEST POINTS
AGND
DGND
-15VA
+15VA
+5VD
MICROPHONE BIAS VOLTAGE SUPPLY
OPTICAL RECORD INPUTS
BYPASS CAPACITORS
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN OPTO/MIC BD,MC12
MIC BIAS & OPTO INPUTS
060-13619
13619-32
SHEET 2 OF 2

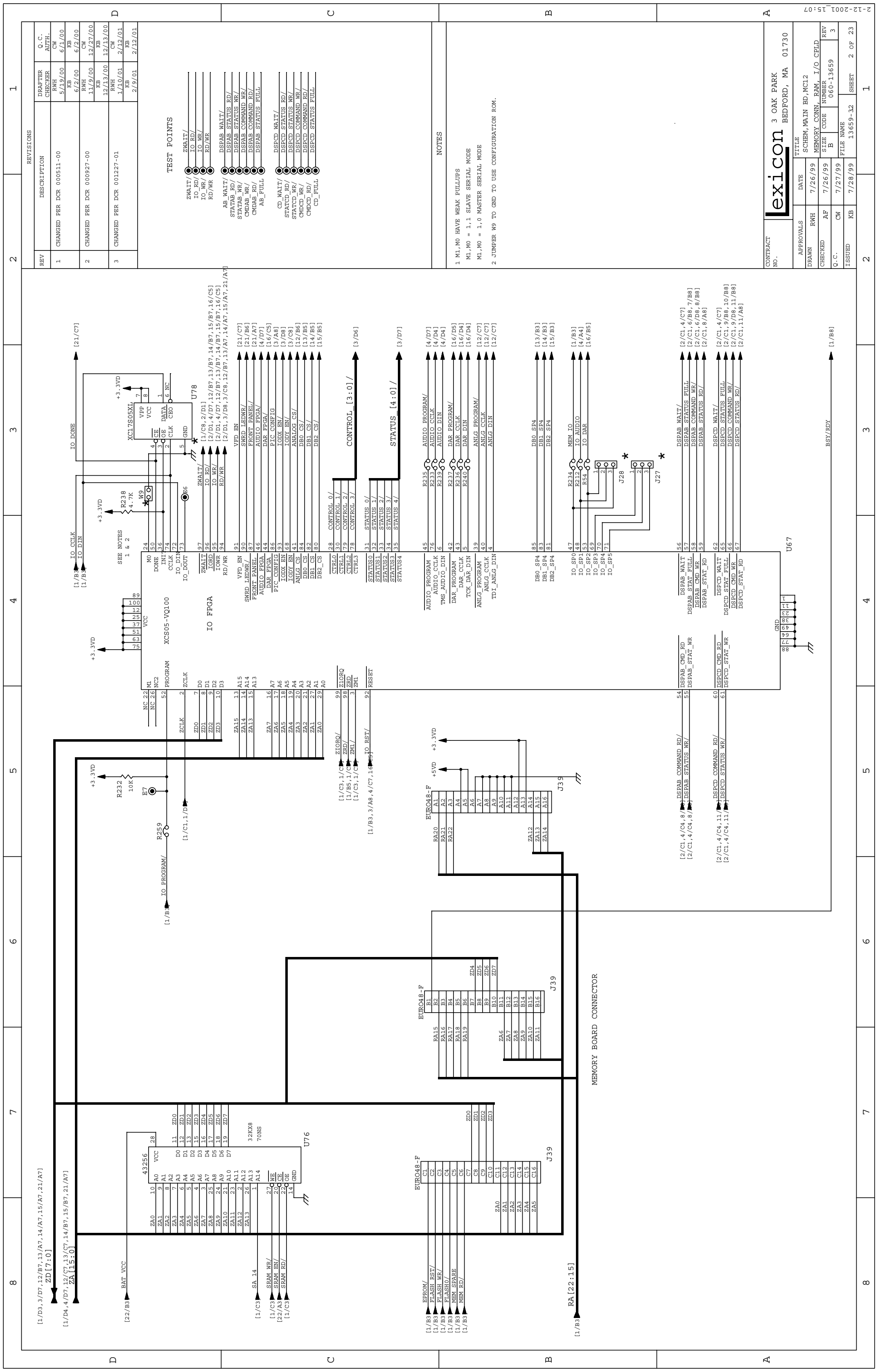
Your Notes:


REVISIONS
REV | DESCRIPTION | DRAFTER CHECKER | Q.C. AUTH.
1 | CHANGED PER DCR 000327-00 | RWH 3/27/00 KB 4/10/00 | CW 4/28/00 KB 4/10/00
2 | CHANGED TITLE PER DCR 000926-00 | RWH 12/5/00 KB 12/5/00 | CW 12/7/00 KB 12/5/00
NOTES
1 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND
2 LAST REFERENCE DESIGNATORS USED: D1, J1, SW1
© 2000 Lexicon, Inc.
CONTRACT NO.
lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE SCHEM,STANDBY BD, MC12
APPROVALS DATE
DRAWN CW 10/27/99
CHECKED KB 10/27/99
Q.C. RWH 10/27/99
ISSUED KB 10/27/99
SIZE B CODE NUMBER 060-13629 REV 2
FILE NAME 13629-21 SHEET 1 OF 1
12-7-2000_16:03
J1
SW1
STANDBY LED
RED
D1

Your Notes:

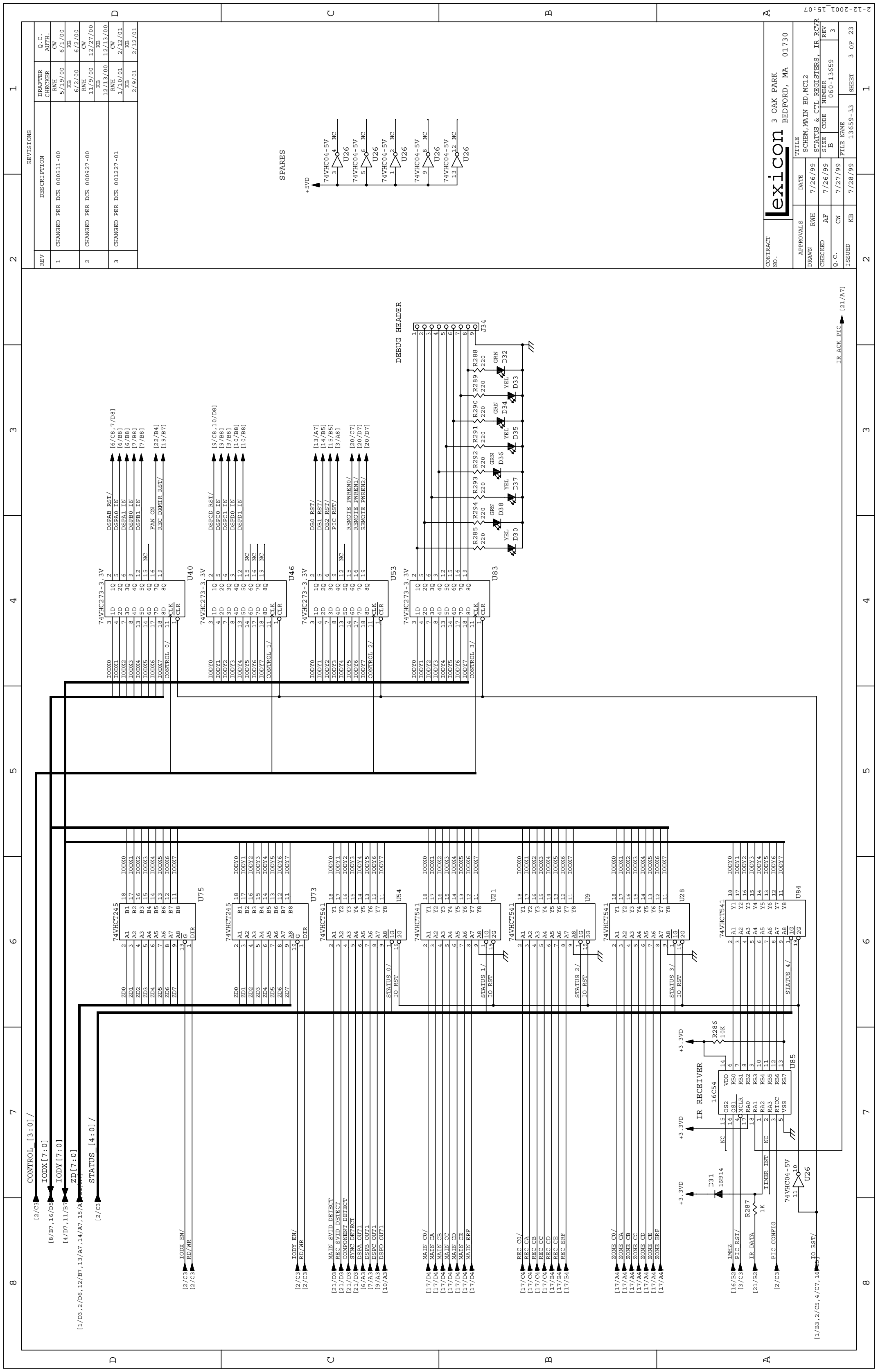


Your Notes:

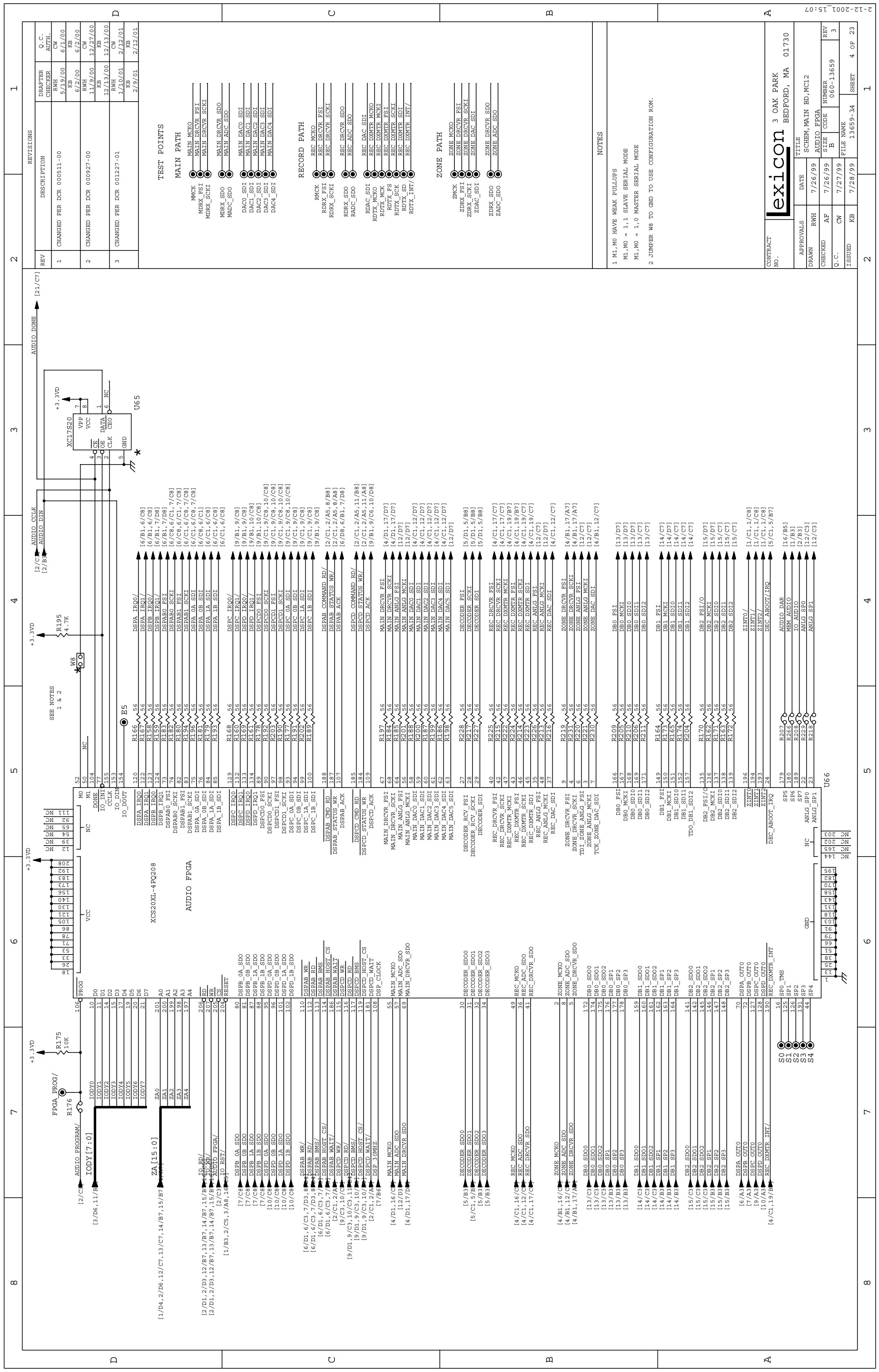


lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
MEMORY CONN,RAM,I/O CPLD
060-13659
13659-32
SHEET 2 OF 23
TEST POINTS
NOTES
IO FPGA
XCS05-VQ100
MEMORY BOARD CONNECTOR

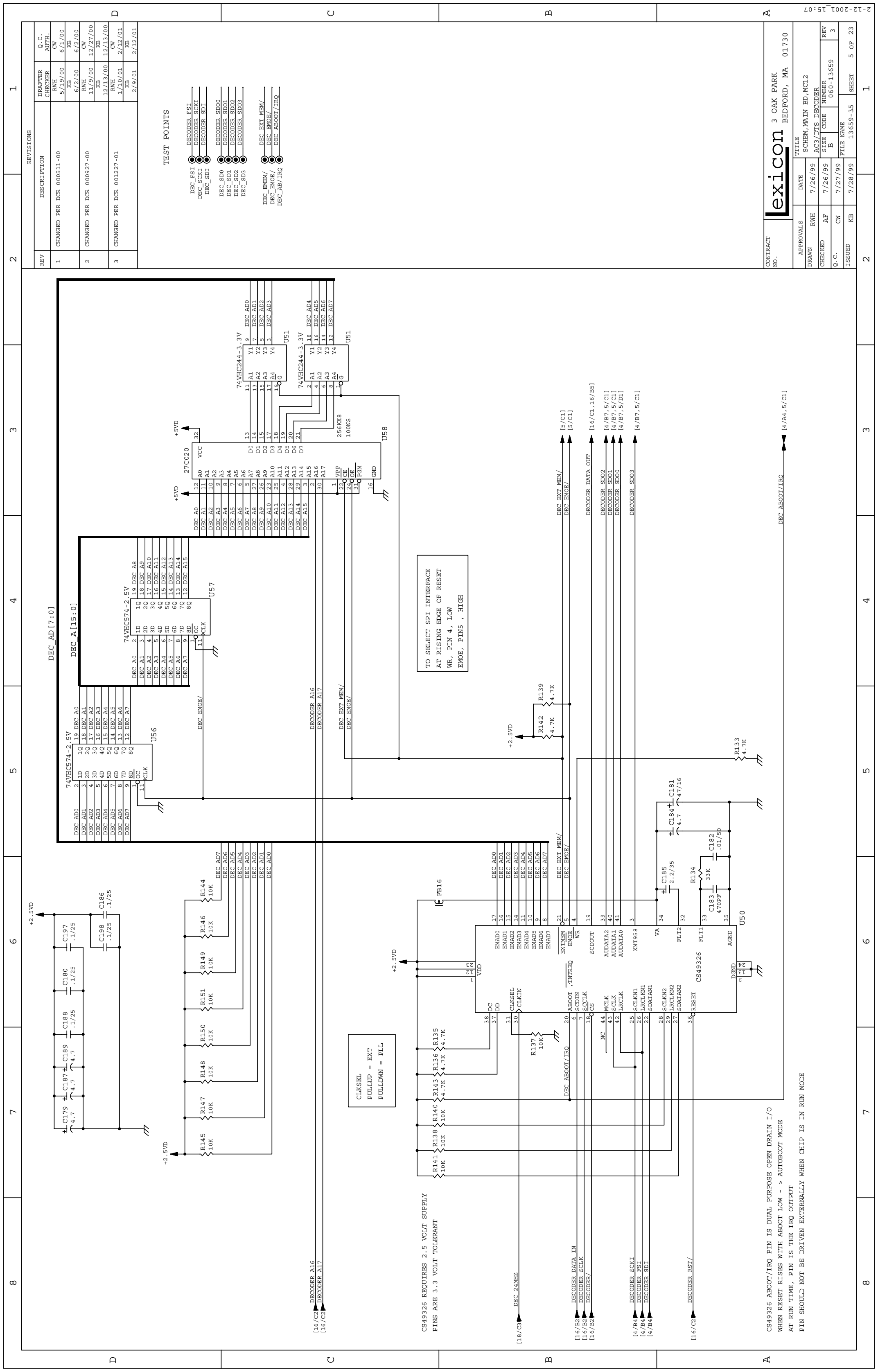
Your Notes:



Your Notes:

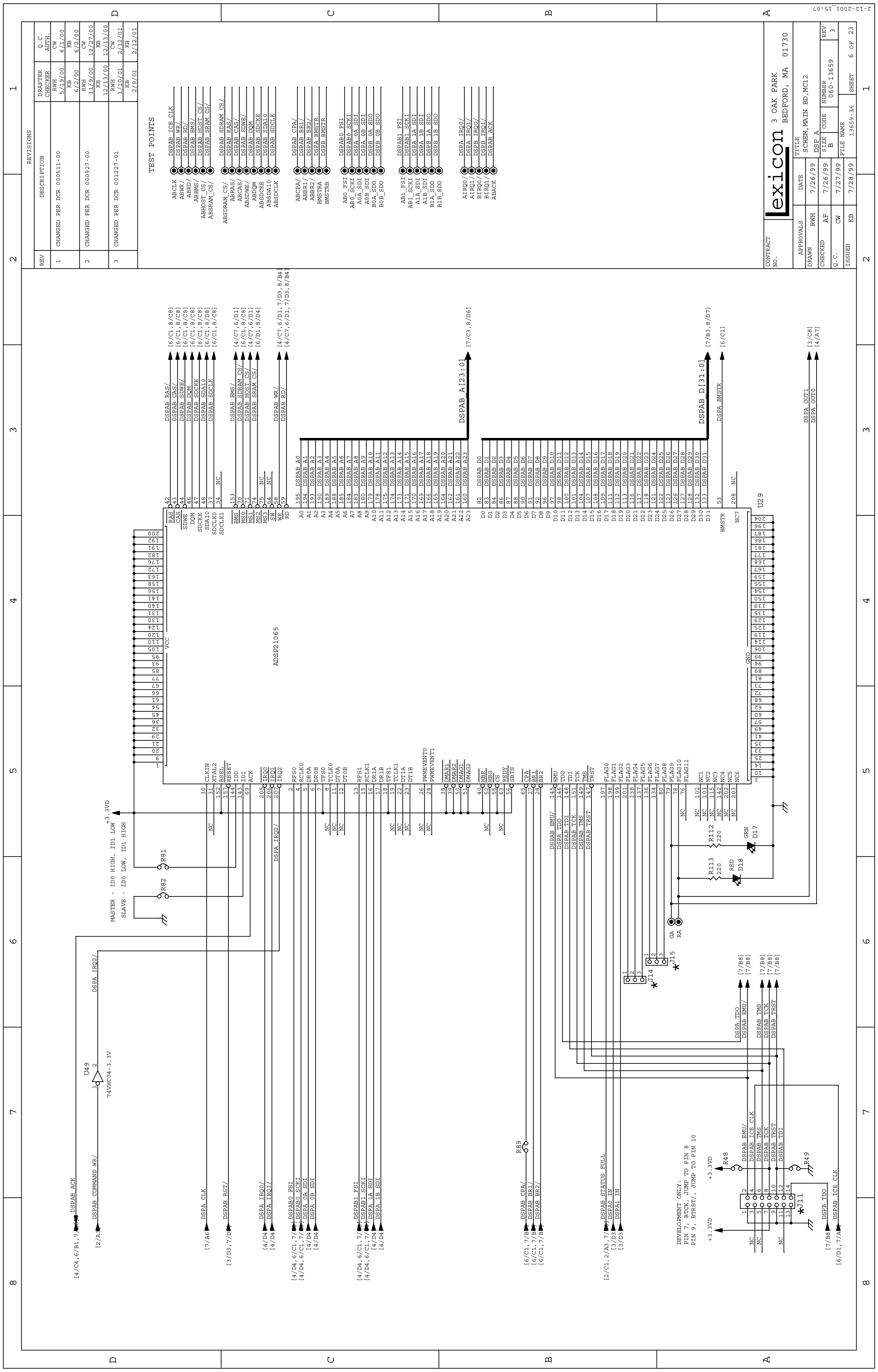


Your Notes:

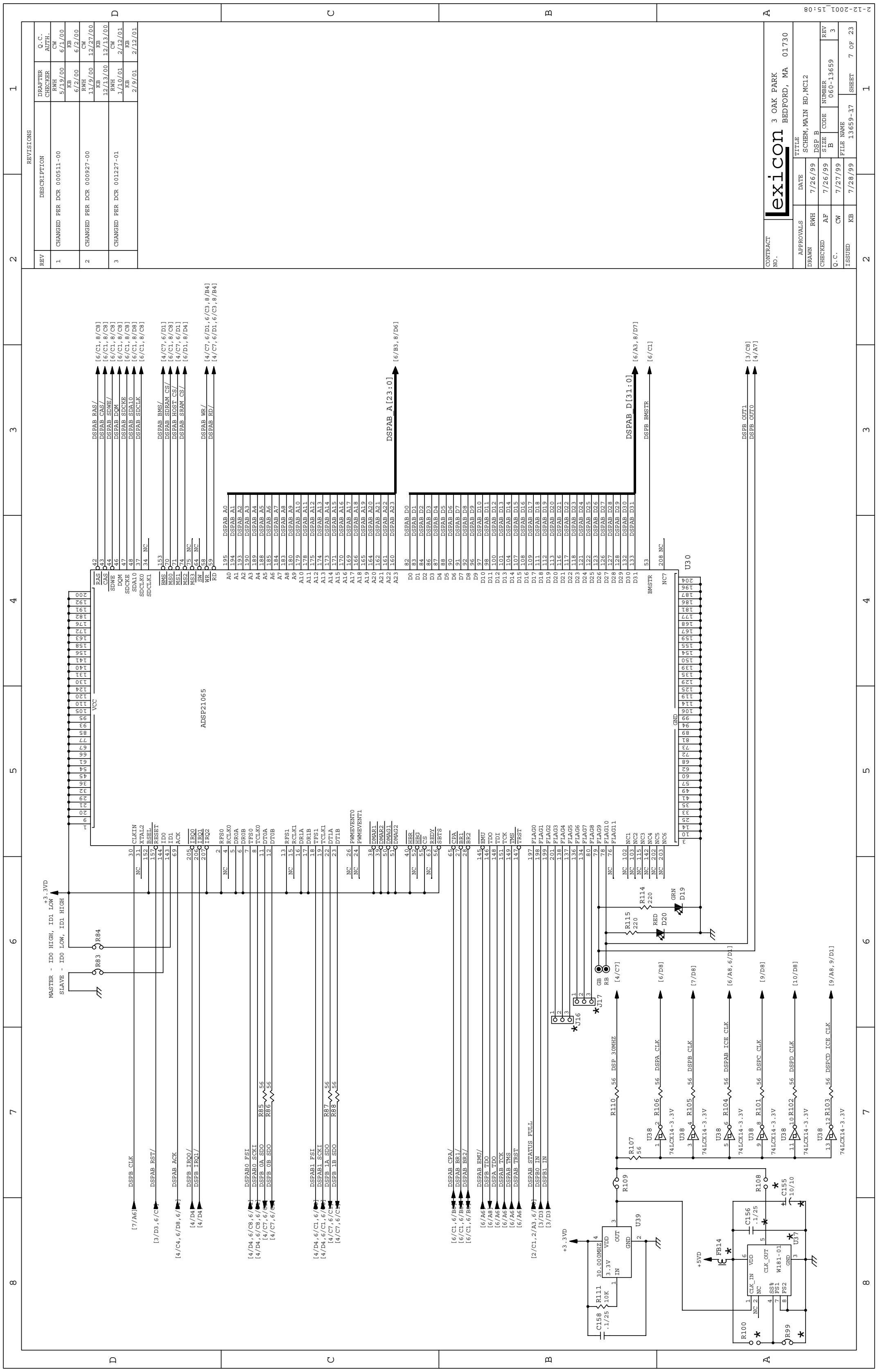


TEST POINTS
lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
AC3/DTS DECODER
060-13659

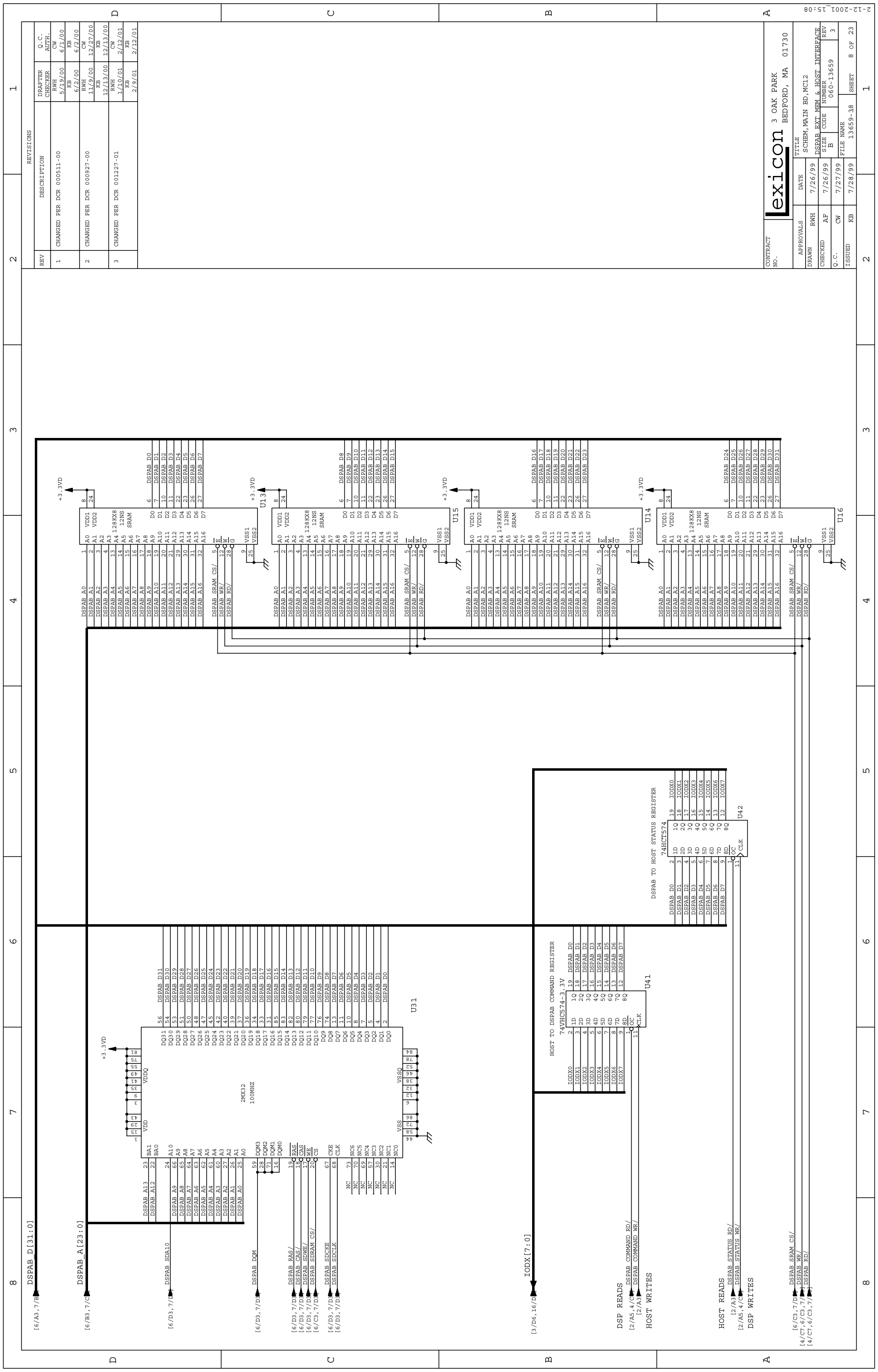
Your Notes:


TEST POINTS
ADSP21065
U29
DSPAB_A[23:0]
DSPAB_D[31:0]
lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
DSP A
060-13659
SHEET 6 OF 23

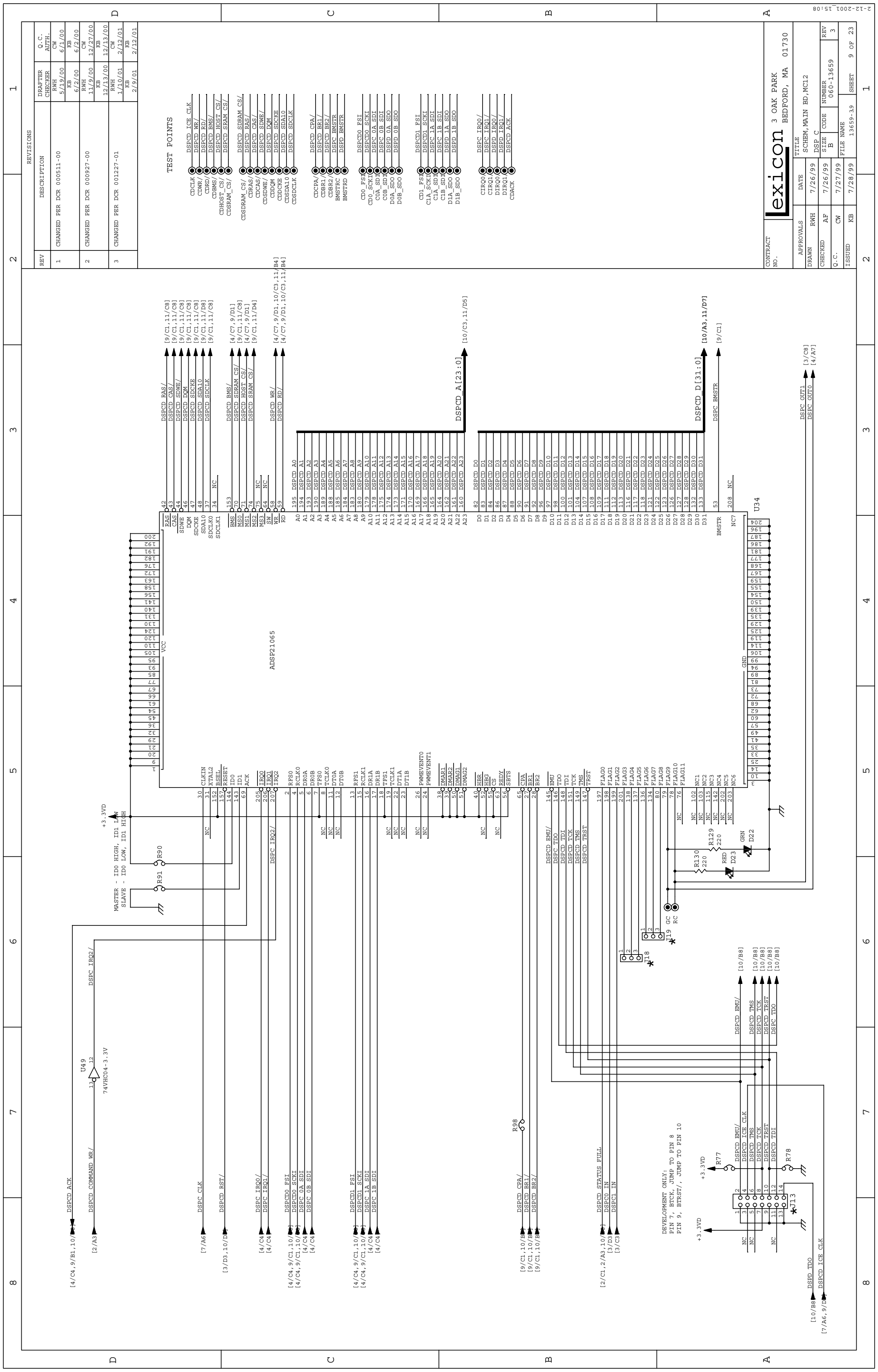
Your Notes:


ADSP21065
DSPAB_A[23:0]
DSPAB_D[31:0]
U30
lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
DSP B
060-13659
13659-37
7 OF 23

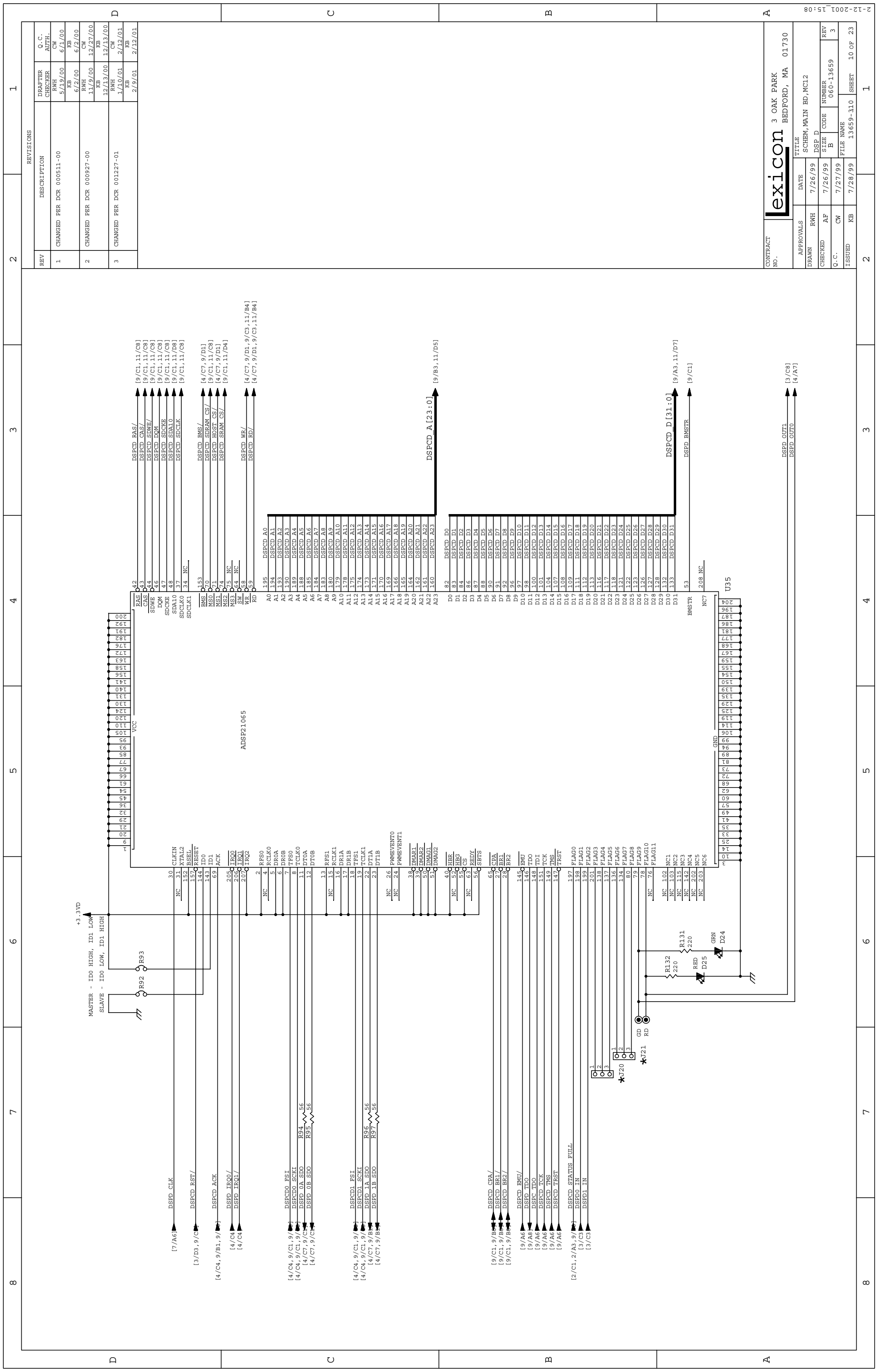
Your Notes:


lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
DSPAB EXT MEM & HOST INTERFACE
060-13659
13659-38
SHEET 8 OF 23
HOST TO DSPAB COMMAND REGISTER
DSPAB TO HOST STATUS REGISTER
DSPAB_D[31:0]
DSPAB_A[23:0]
IODX[7:0]
DSP READS
HOST WRITES
HOST READS
DSP WRITES

Your Notes:

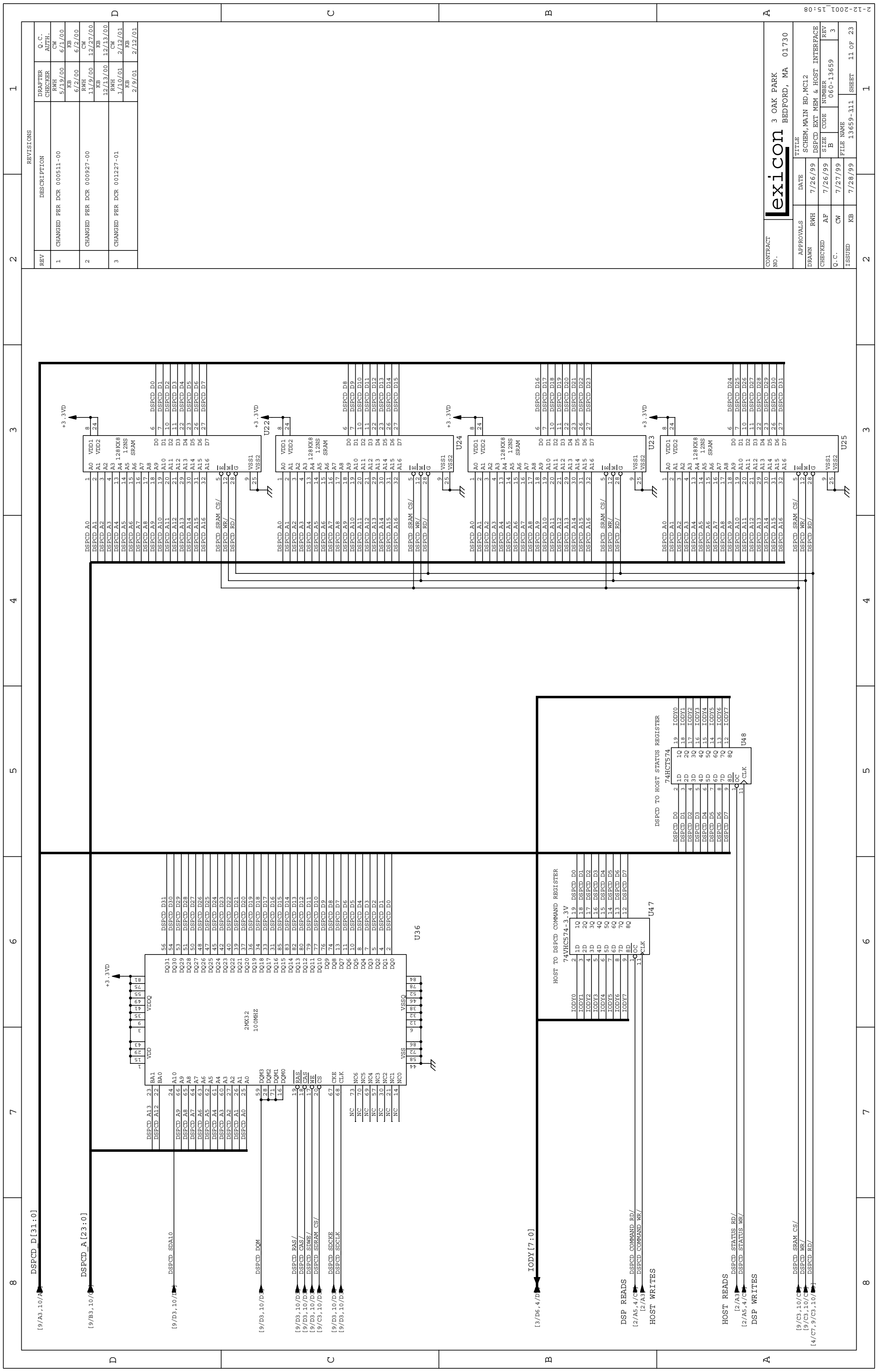

REVISIONS
TEST POINTS
ADSP21065
U34
lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
DSP C
060-13659
SHEET 9 OF 23

Your Notes:

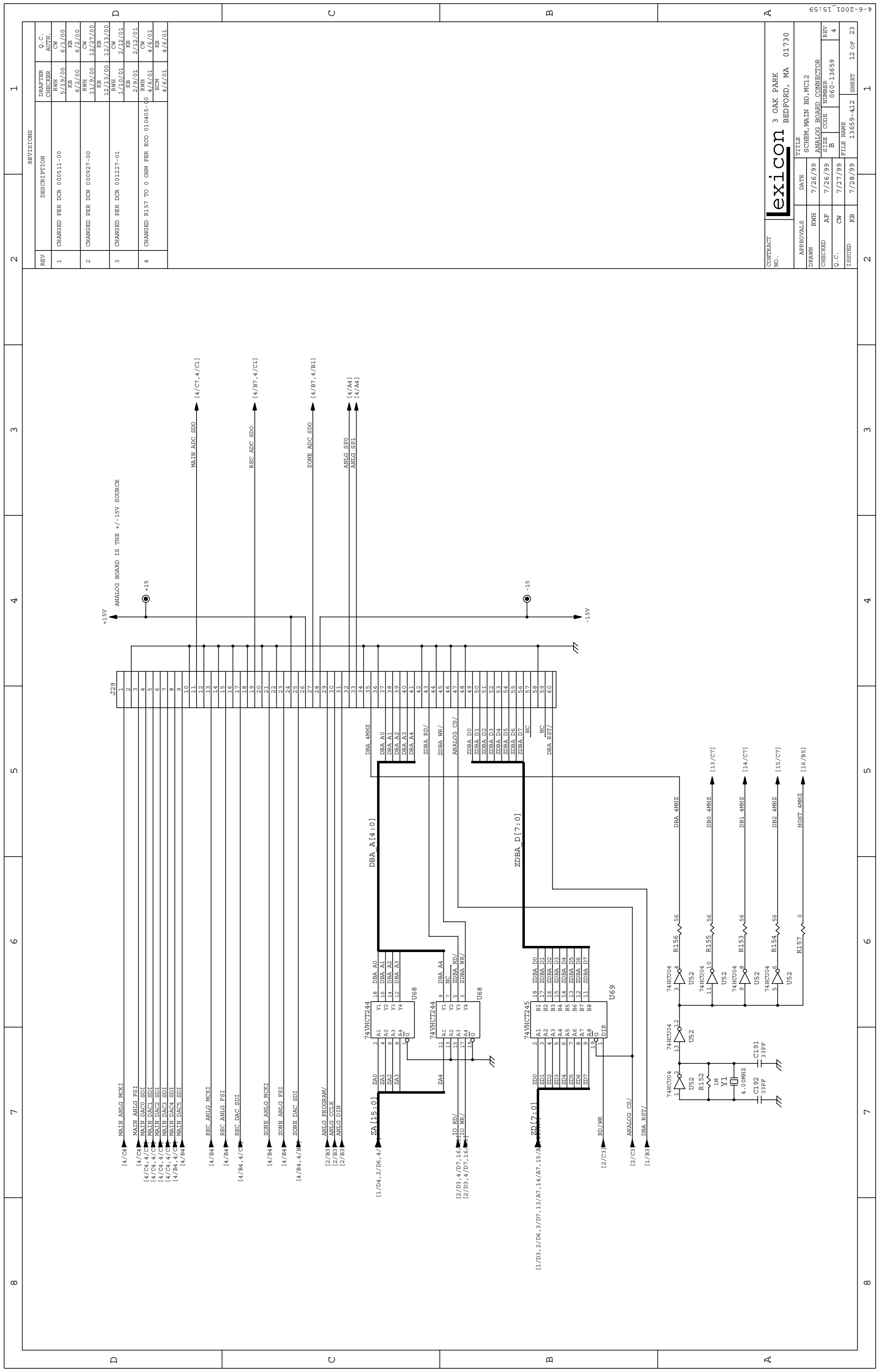


REVISIONS
REV DESCRIPTION DRAFTER CHECKER Q.C. AUTH.
1 CHANGED PER DCR 000511-00 RWH 5/19/00 CW 6/1/00 KB 6/2/00 KB 6/2/00
2 CHANGED PER DCR 000927-00 RWH 11/9/00 CW 12/27/00 KB 12/13/00 KB 12/11/00
3 CHANGED PER DCR 001227-01 RWH 1/10/01 CW 2/12/01 KB 2/9/01 KB 2/12/01
lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE SCHEM,MAIN BD,MC12 DSP D
APPROVALS DATE
DRAWN RWH 7/26/99
CHECKED AP 7/26/99
Q.C. CW 7/27/99
ISSUED KB 7/28/99
SIZE B CODE NUMBER 060-13659 REV 3
FILE NAME 13659-310 SHEET 10 OF 23
ADSP21065
U35
DSPCD A[23:0]
DSPCD D[31:0]
MASTER - ID0 HIGH, ID1 LOW
SLAVE - ID0 LOW, ID1 HIGH
+3.3VD

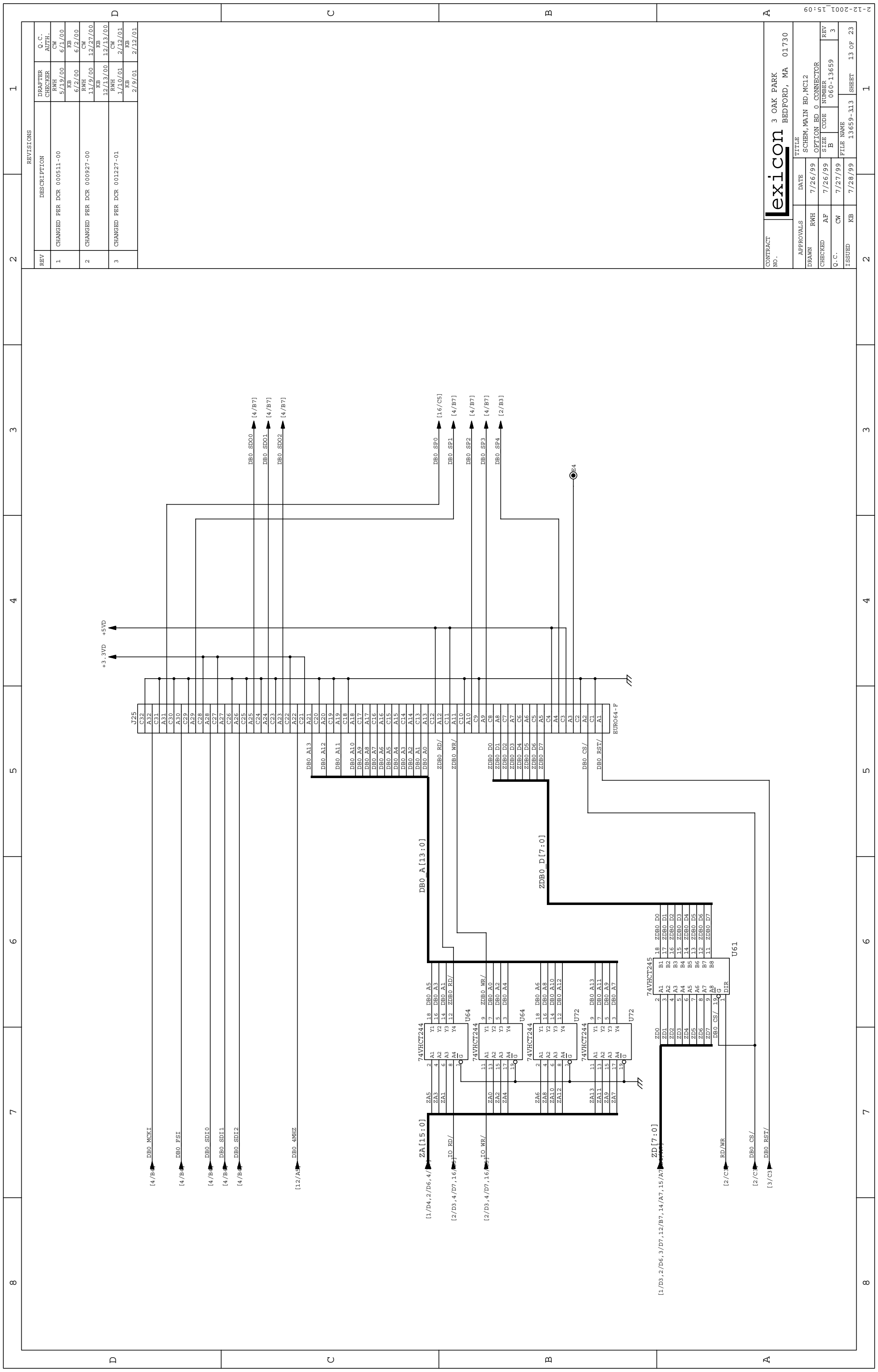
Your Notes:


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
DSPCD EXT MEM & HOST INTERFACE
060-13659
13659-311
11 OF 23
U36
U22
U23
U24
U25
U47
U48
DSPCD_D[31:0]
DSPCD_A[23:0]
IODY[7:0]
DSP READS
HOST WRITES
HOST READS
DSP WRITES

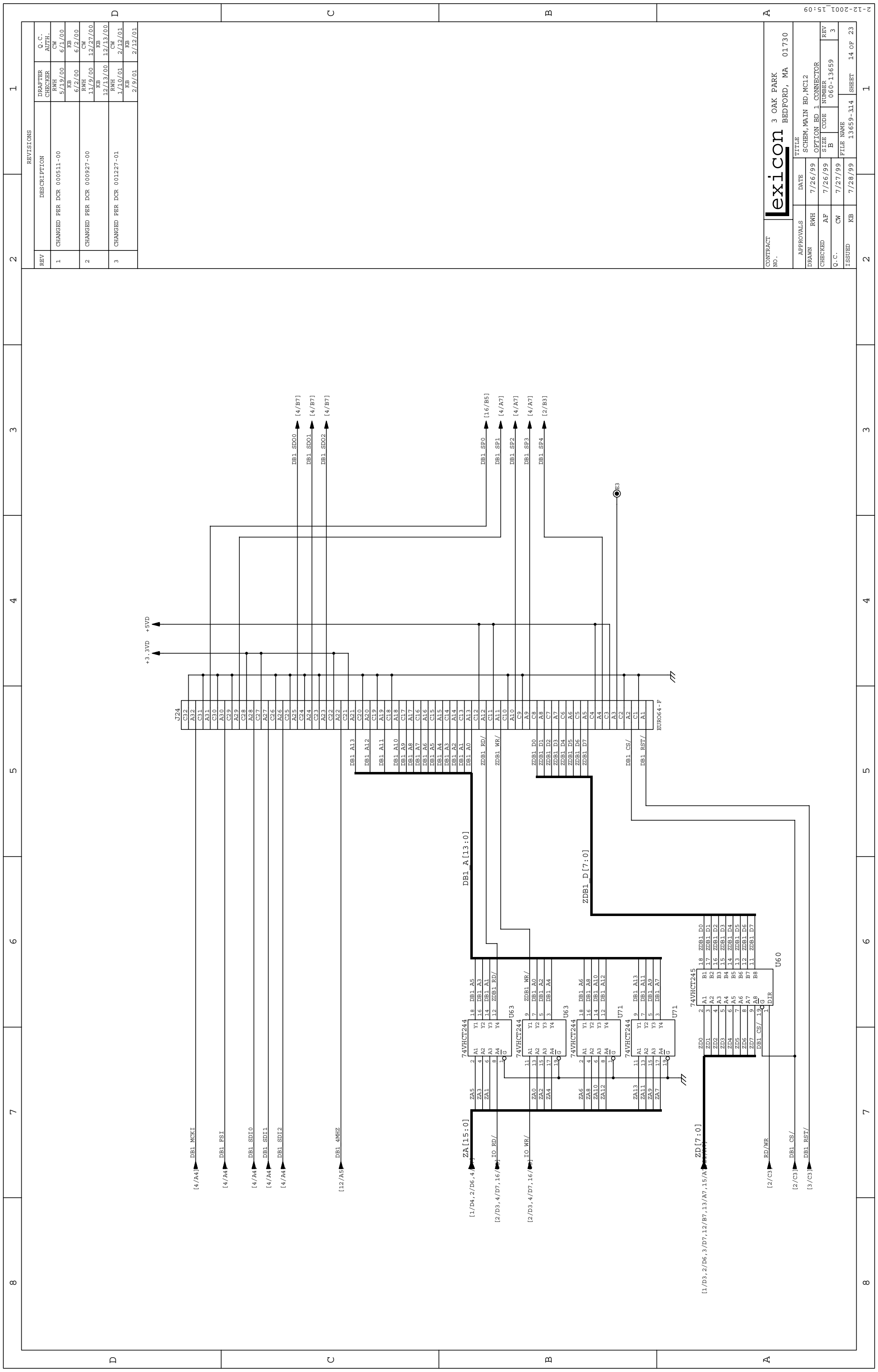
Your Notes:


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
ANALOG BOARD CONNECTOR
060-13659
REV 4
13659-412
SHEET 12 OF 23
J29
U68
U69
74VHCT244
74VHCT245
ANALOG BOARD IS THE +/-15V SOURCE

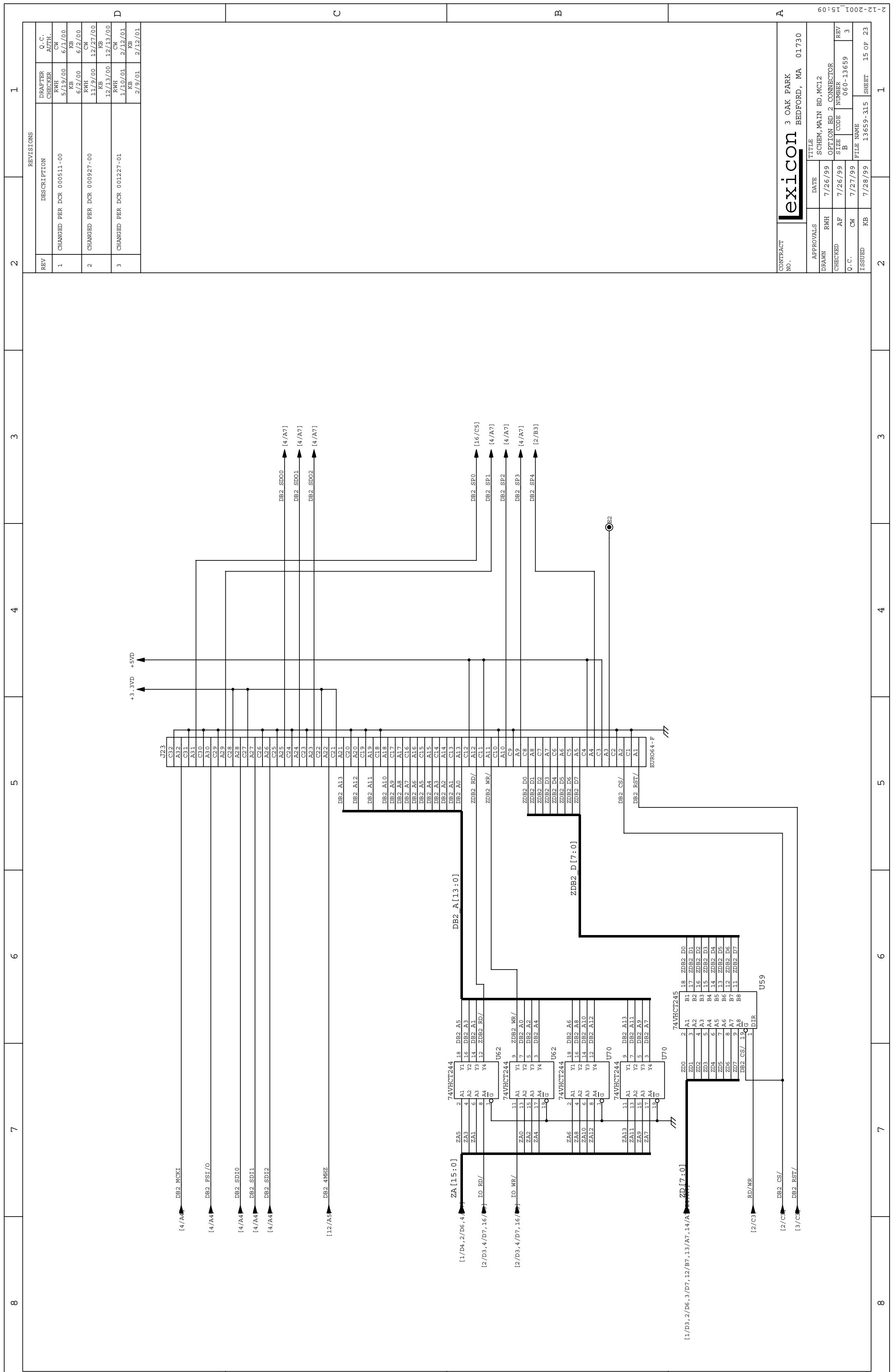
Your Notes:


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
OPTION BD 0 CONNECTOR
060-13659
13659-313
SHEET 13 OF 23

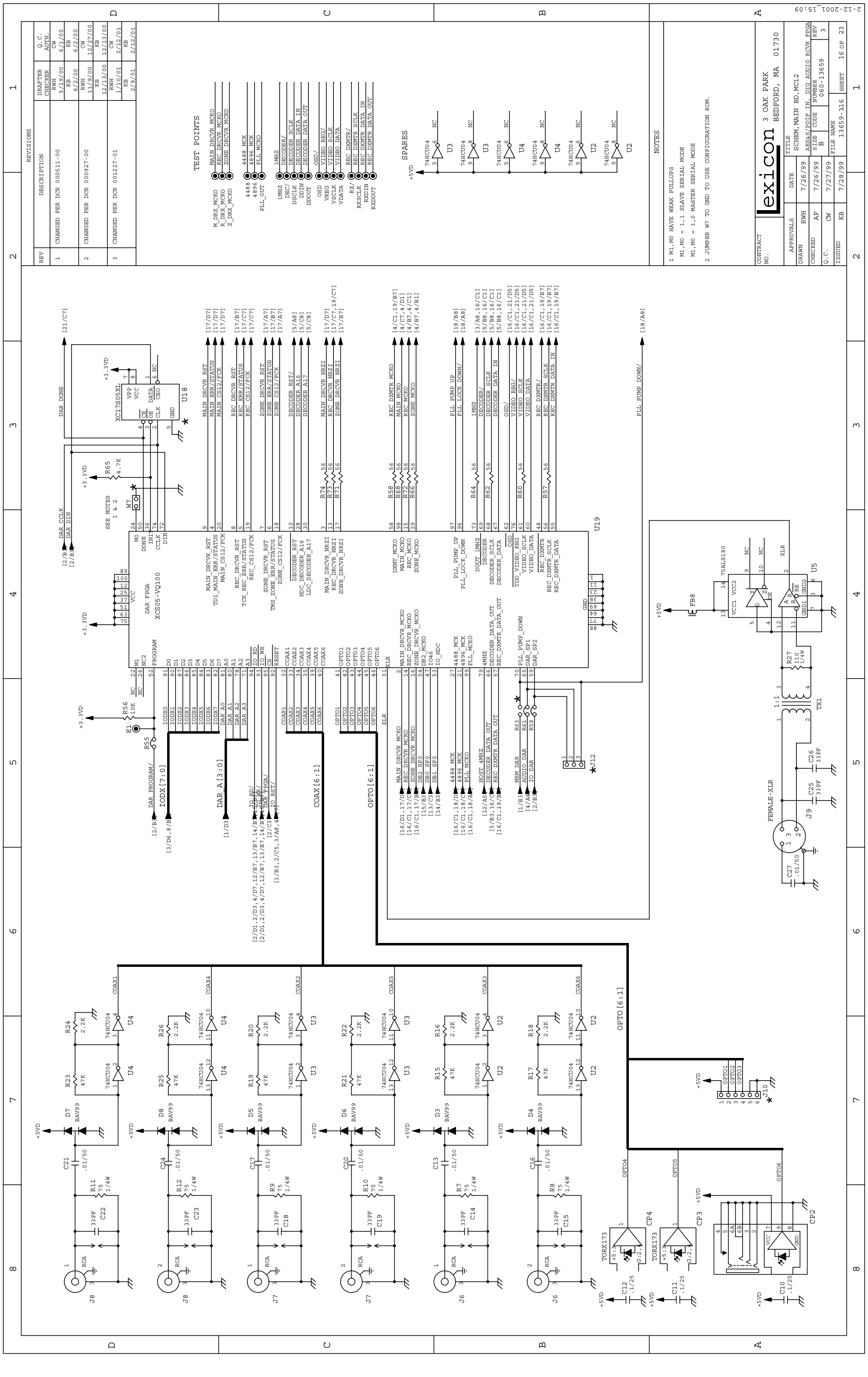
Your Notes:


lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
OPTION BD 1 CONNECTOR
060-13659
13659-314
SHEET 14 OF 23
J24
EURO64-F
74VHCT244
74VHCT245
U63
U71
U60
DB1 A[13:0]
ZDB1 D[7:0]
ZA[15:0]
ZD[7:0]

Your Notes:

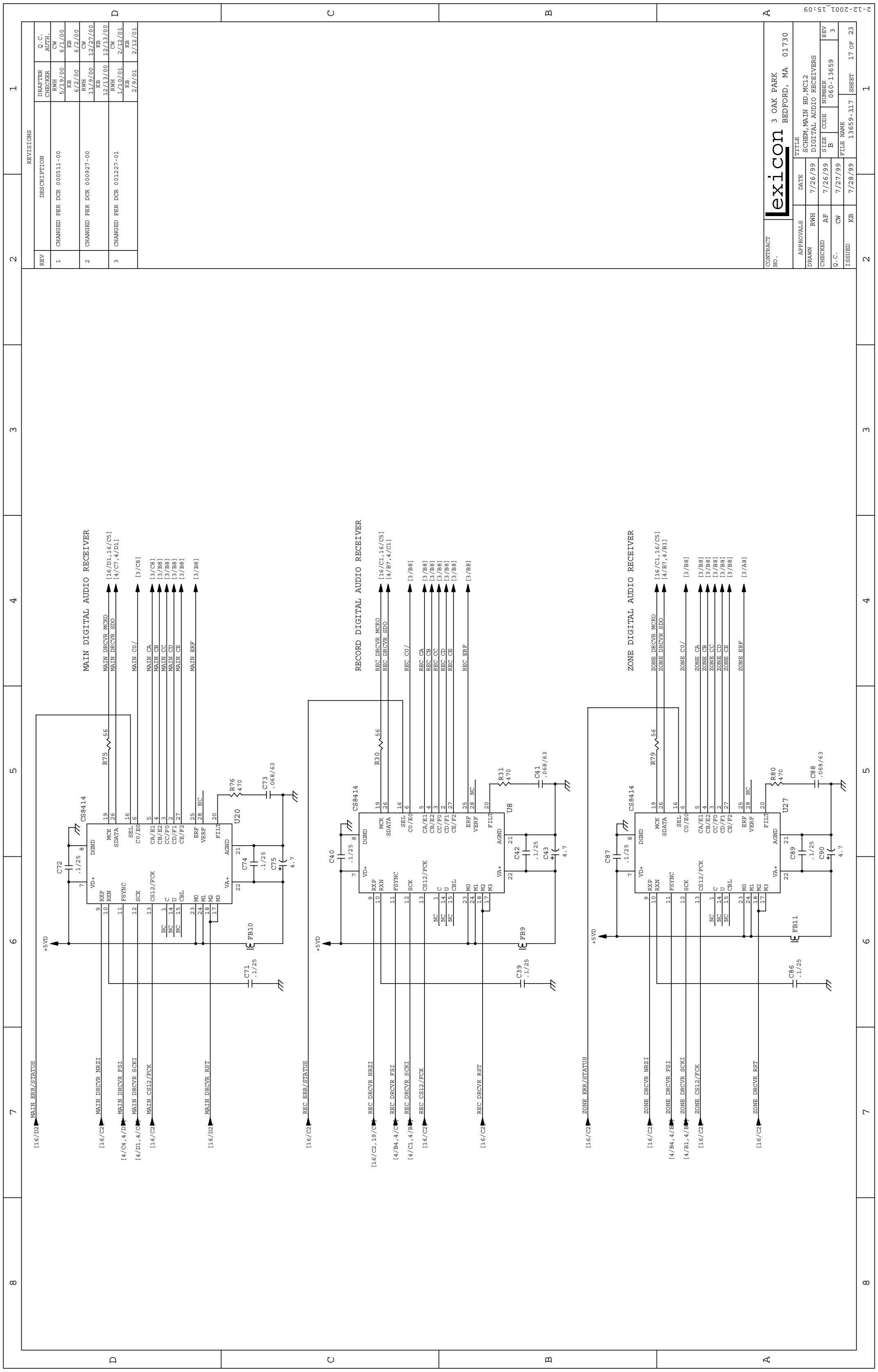

lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
OPTION BD 2 CONNECTOR
060-13659
13659-315
SHEET 15 OF 23
REVISIONS
CHANGED PER DCR 000511-00
CHANGED PER DCR 000927-00
CHANGED PER DCR 001227-01
J23
EURO64-F
74VHCT244
74VHCT245
U59
U62
U70
DB2_A[13:0]
ZDB2_D[7:0]
ZA[15:0]
ZD[7:0]
+3.3VD
+5VD

Your Notes:

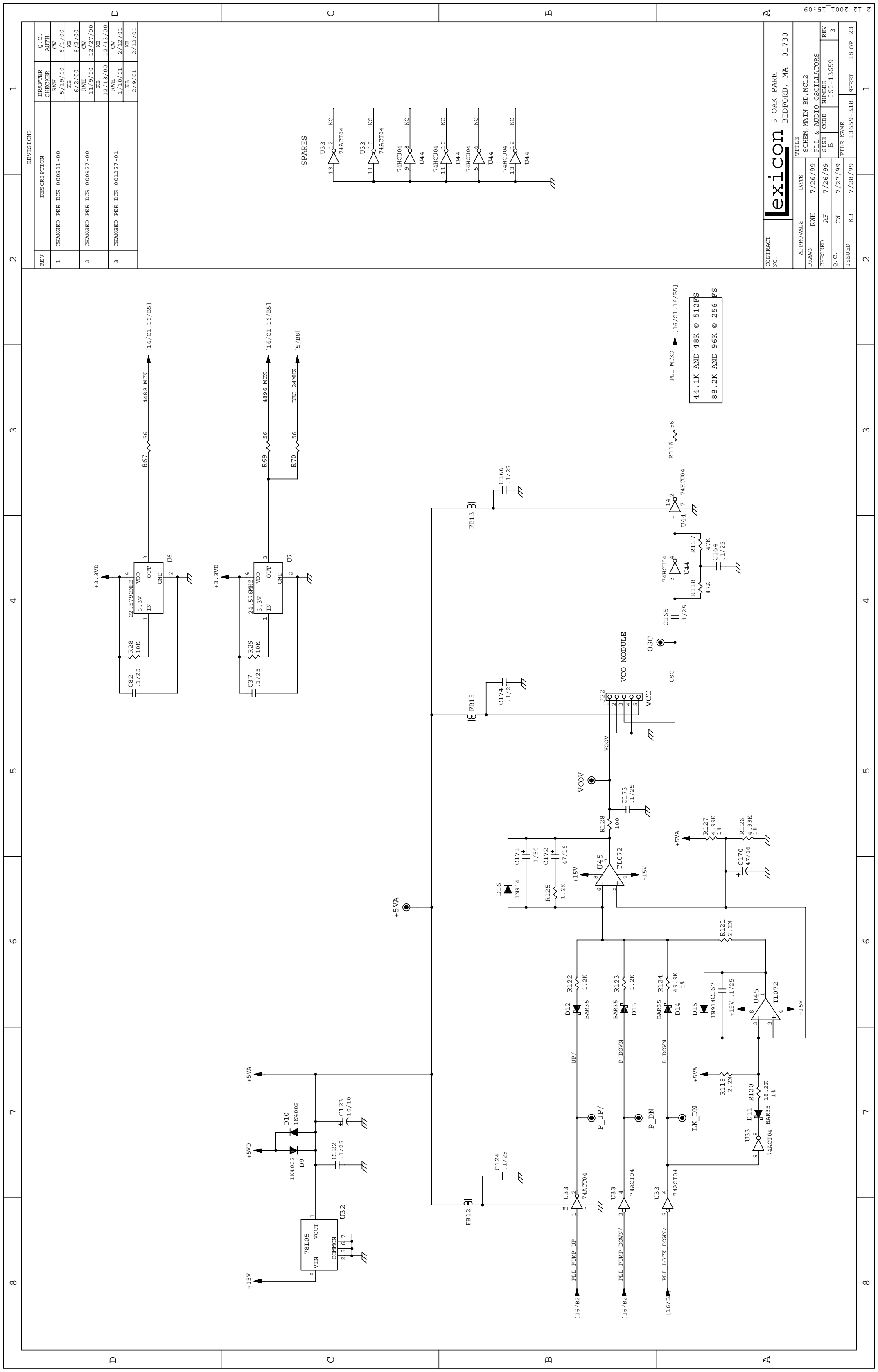


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
060-13659
13659-316
SHEET 16 OF 23

Your Notes:

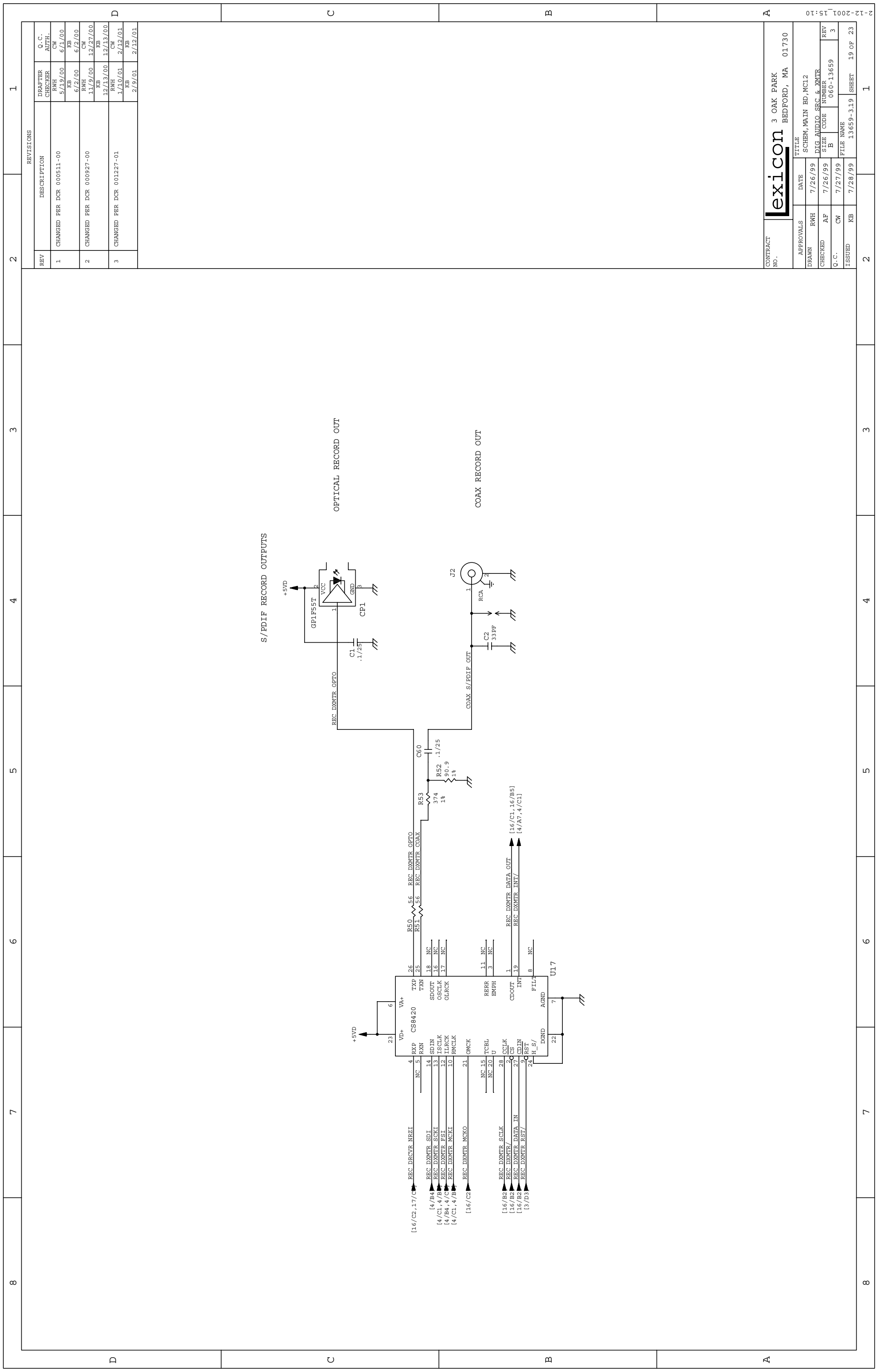

MAIN DIGITAL AUDIO RECEIVER
RECORD DIGITAL AUDIO RECEIVER
ZONE DIGITAL AUDIO RECEIVER
CS8414
U20
U8
U27
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
DIGITAL AUDIO RECEIVERS
060-13659
13659-317
SHEET 17 OF 23

Your Notes:

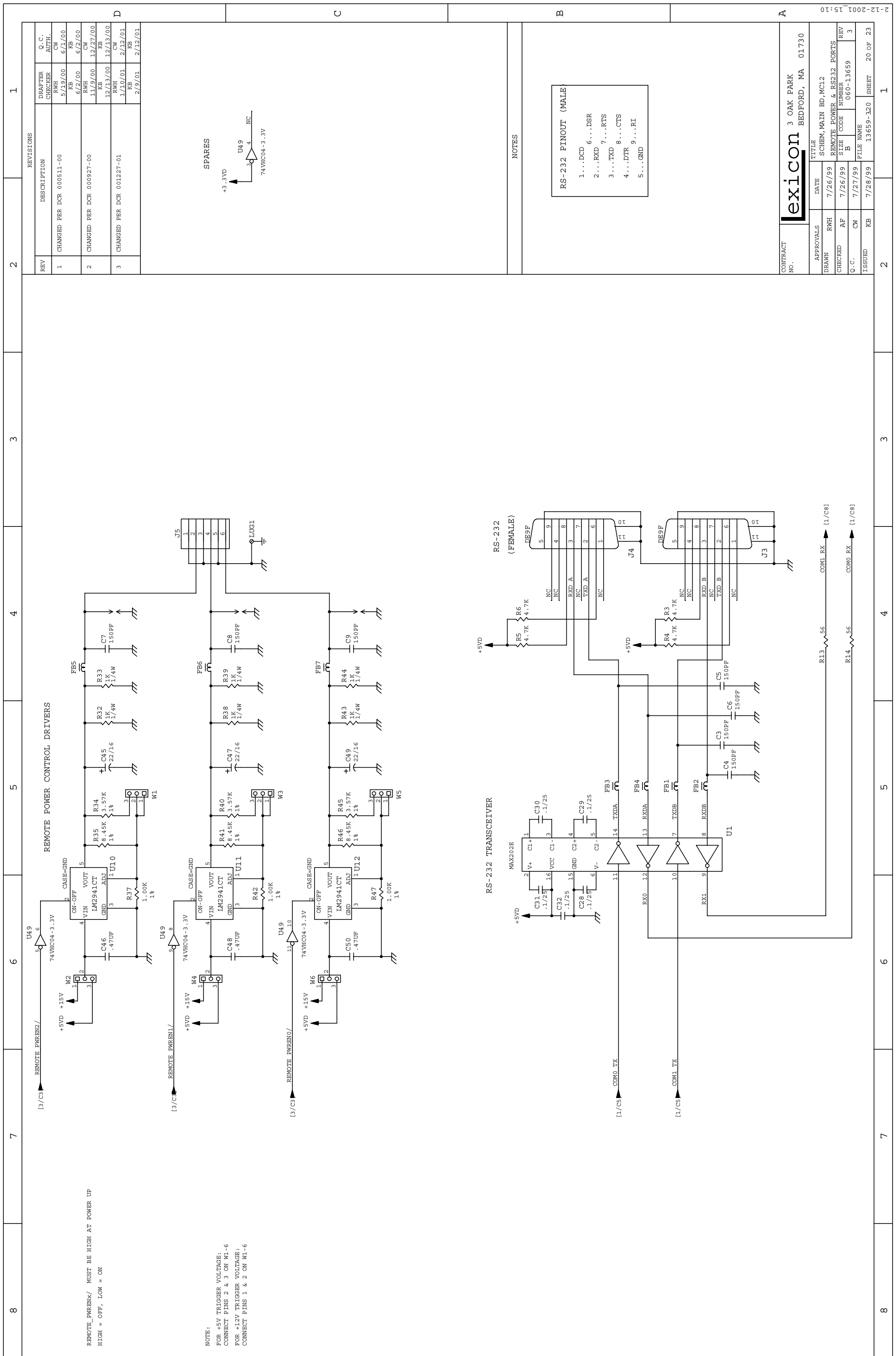


lexicon
3 OAK PARK
BEDFORD, MA 01730
TITLE
SCHEM,MAIN BD,MC12
PLL & AUDIO OSCILLATORS
NUMBER
060-13659
FILE NAME
13659-318
SHEET 18 OF 23
REVISIONS
CHANGED PER DCR 000511-00
CHANGED PER DCR 000927-00
CHANGED PER DCR 001227-01
SPARES
VCO MODULE
44.1K AND 48K @ 512FS
88.2K AND 96K @ 256 FS
PLL MCKO
4488 MCK
4896 MCK
OSC 24MHZ
P_UP/
P_DN
LK_DN
VCOV
OSC
+5VA

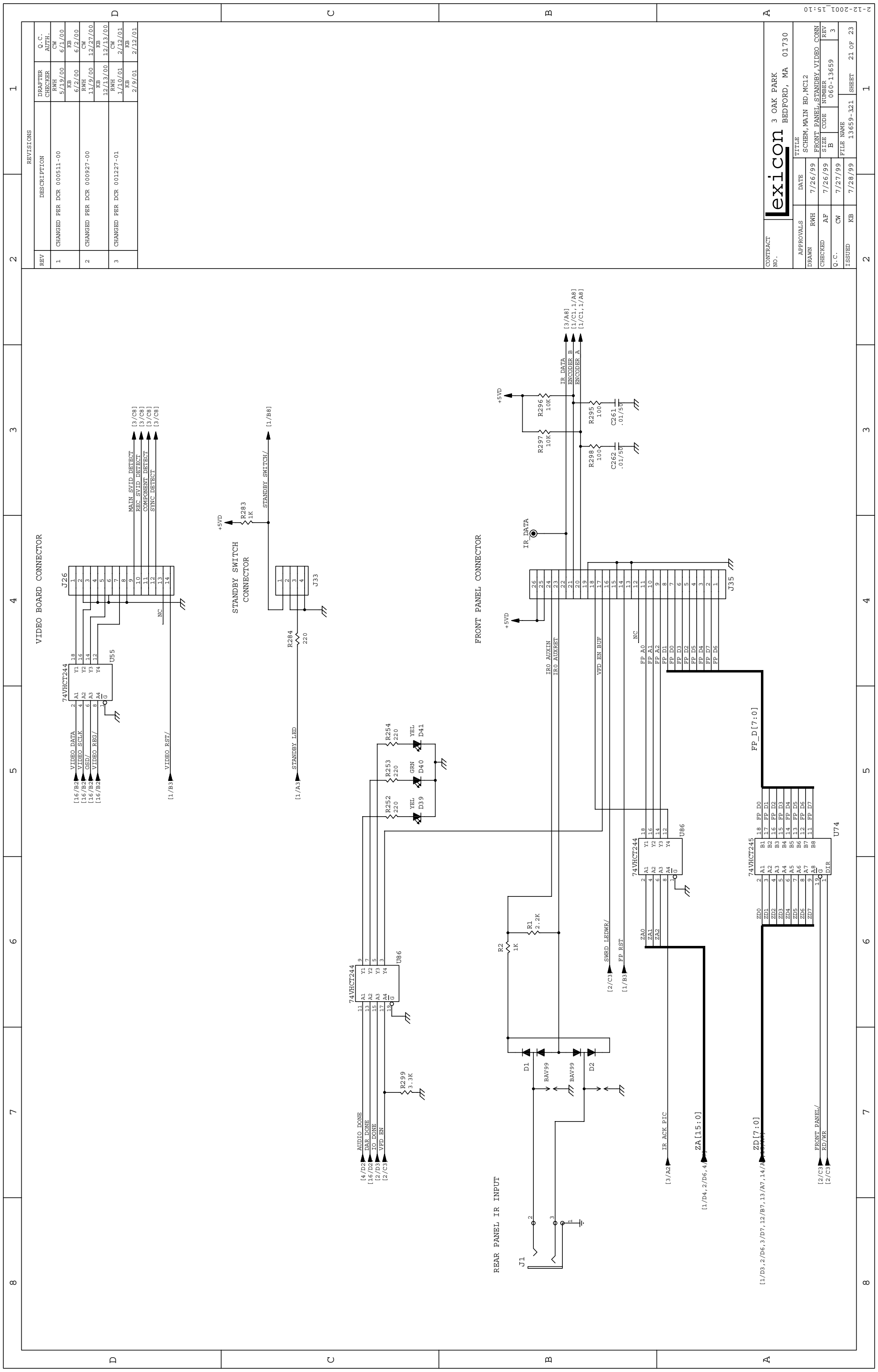
Your Notes:


S/PDIF RECORD OUTPUTS
OPTICAL RECORD OUT
COAX RECORD OUT
GP1F55T
CP1
J2
RCA
CS8420
U17
REVISIONS
CHANGED PER DCR 000511-00
CHANGED PER DCR 000927-00
CHANGED PER DCR 001227-01
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
DIG AUDIO SRC & XMTR
060-13659
13659-3.19
19 OF 23

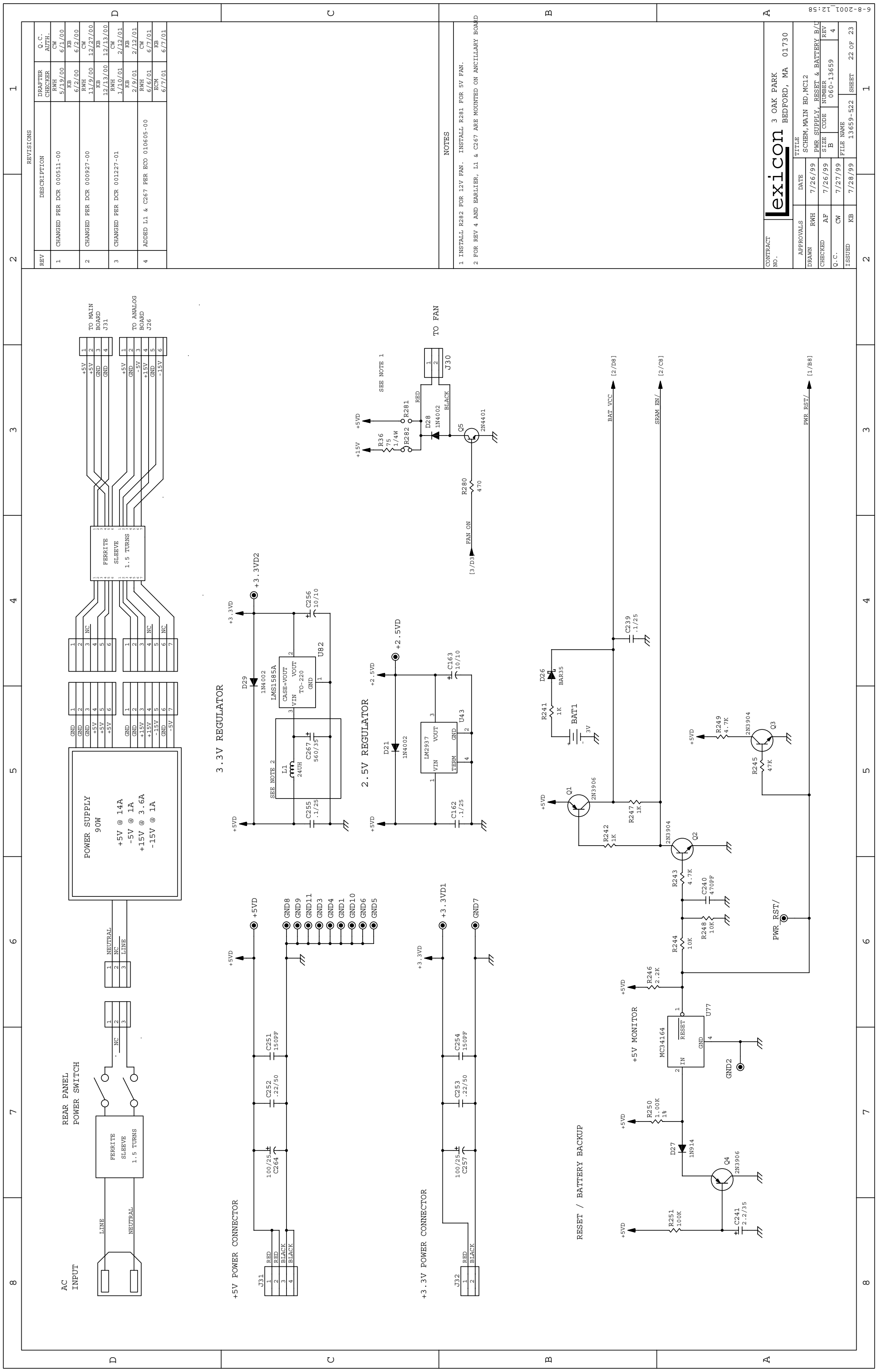
Your Notes:


REVISIONS
SPARES
NOTES
RS-232 PINOUT (MALE)
1...DCD 6...DSR
2...RXD 7...RTS
3...TXD 8...CTS
4...DTR 9...RI
5...GND
REMOTE POWER CONTROL DRIVERS
RS-232 TRANSCEIVER
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
REMOTE POWER & RS232 PORTS
060-13659
13659-320
20 OF 23

Your Notes:

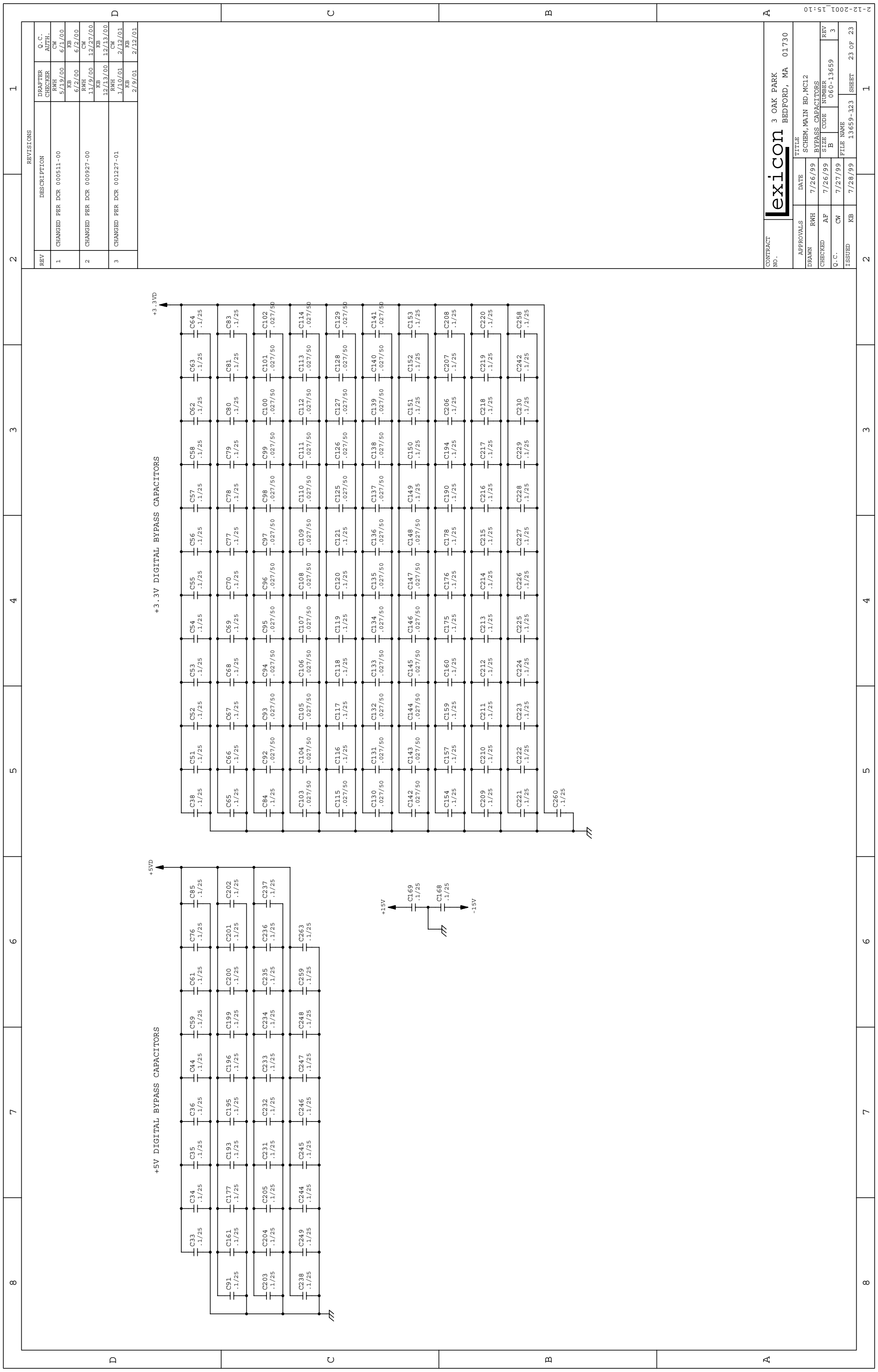

VIDEO BOARD CONNECTOR
STANDBY SWITCH CONNECTOR
FRONT PANEL CONNECTOR
REAR PANEL IR INPUT
J26
J33
J35
J1
U55
U86
U74
74VHCT244
74VHCT245
FP_D[7:0]
ZA[15:0]
ZD[7:0]
lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE SCHEM,MAIN BD,MC12 FRONT PANEL,STANDBY,VIDEO CONN
SIZE B
NUMBER 060-13659
REV 3
FILE NAME 13659-321
SHEET 21 OF 23
REVISIONS
1 CHANGED PER DCR 000511-00
2 CHANGED PER DCR 000927-00
3 CHANGED PER DCR 001227-01

Your Notes:

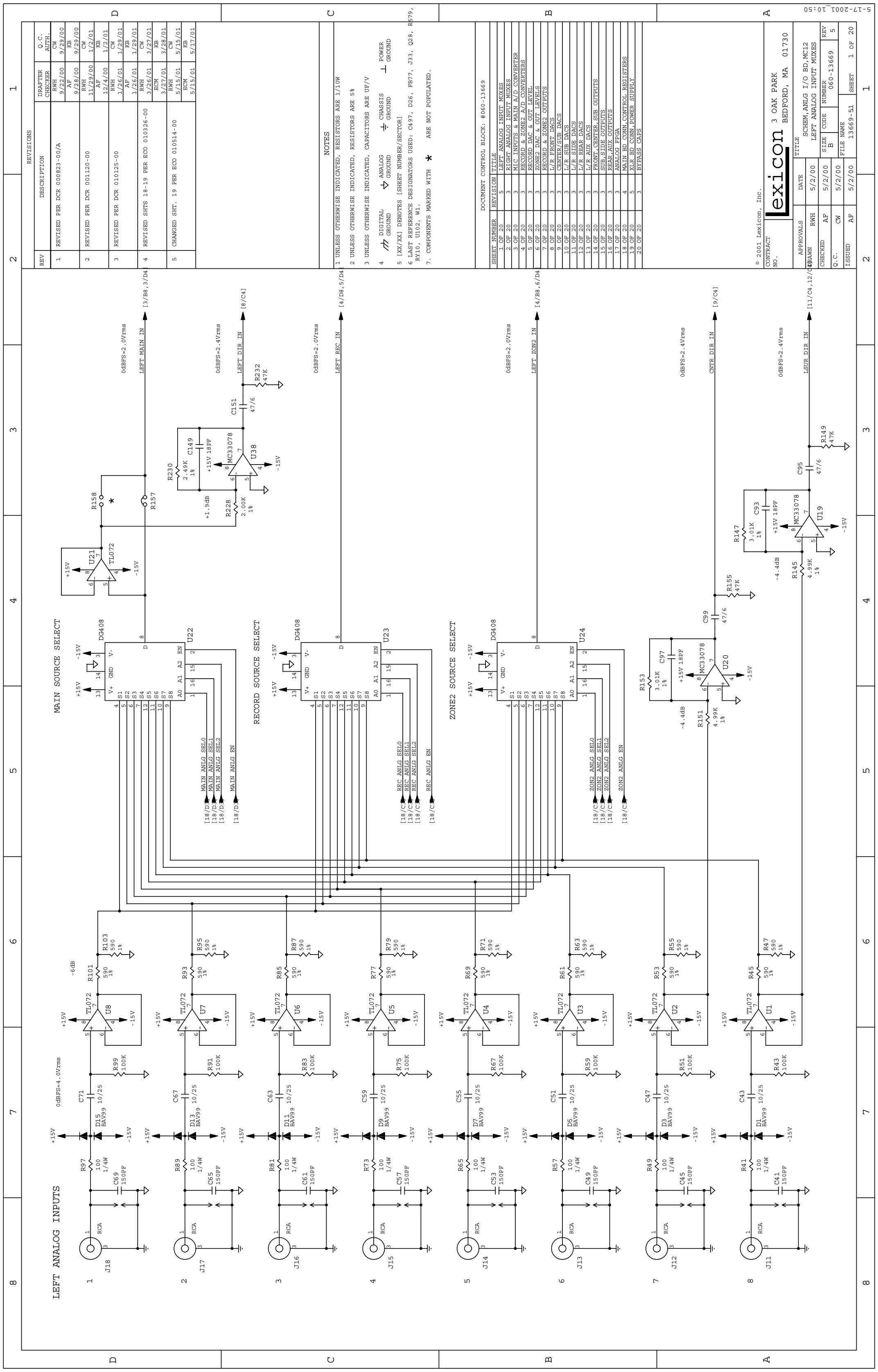


REVISIONS
REV | DESCRIPTION | DRAFTER CHECKER | Q.C. AUTH.
1 CHANGED PER DCR 000511-00
2 CHANGED PER DCR 000927-00
3 CHANGED PER DCR 001227-01
4 ADDED L1 & C267 PER ECO 010605-00
NOTES
1 INSTALL R282 FOR 12V FAN. INSTALL R281 FOR 5V FAN.
2 FOR REV 4 AND EARLIER, L1 & C267 ARE MOUNTED ON ANCILLARY BOARD
AC INPUT
REAR PANEL POWER SWITCH
FERRITE SLEEVE 1.5 TURNS
POWER SUPPLY 90W
+5V @ 14A
-5V @ 1A
+15V @ 3.6A
-15V @ 1A
TO MAIN BOARD J31
TO ANALOG BOARD J26
3.3V REGULATOR
2.5V REGULATOR
+5V POWER CONNECTOR
+3.3V POWER CONNECTOR
TO FAN
RESET / BATTERY BACKUP
+5V MONITOR
lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE SCHEM,MAIN BD,MC12 PWR SUPPLY, RESET & BATTERY B/U
SIZE B
NUMBER 060-13659
REV 4
FILE NAME 13659-S22
SHEET 22 OF 23
DRAWN RWH 7/26/99
CHECKED AP 7/26/99
Q.C. CW 7/27/99
ISSUED KB 7/28/99
6-8-2001_12:58

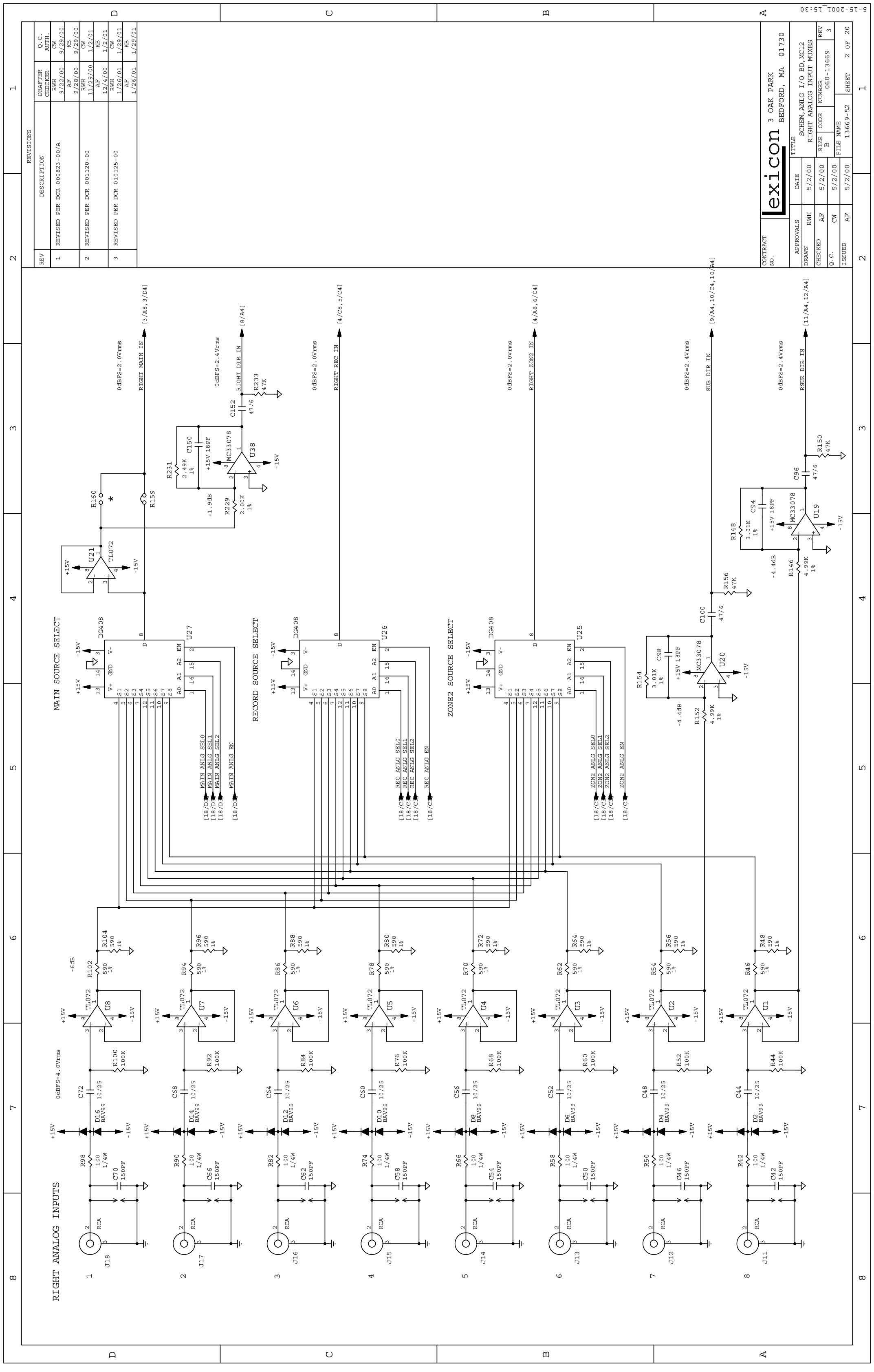
Your Notes:


+3.3V DIGITAL BYPASS CAPACITORS
+5V DIGITAL BYPASS CAPACITORS
REVISIONS
CHANGED PER DCR 000511-00
CHANGED PER DCR 000927-00
CHANGED PER DCR 001227-01
lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,MAIN BD,MC12
BYPASS CAPACITORS
060-13659
13659-323
SHEET 23 OF 23

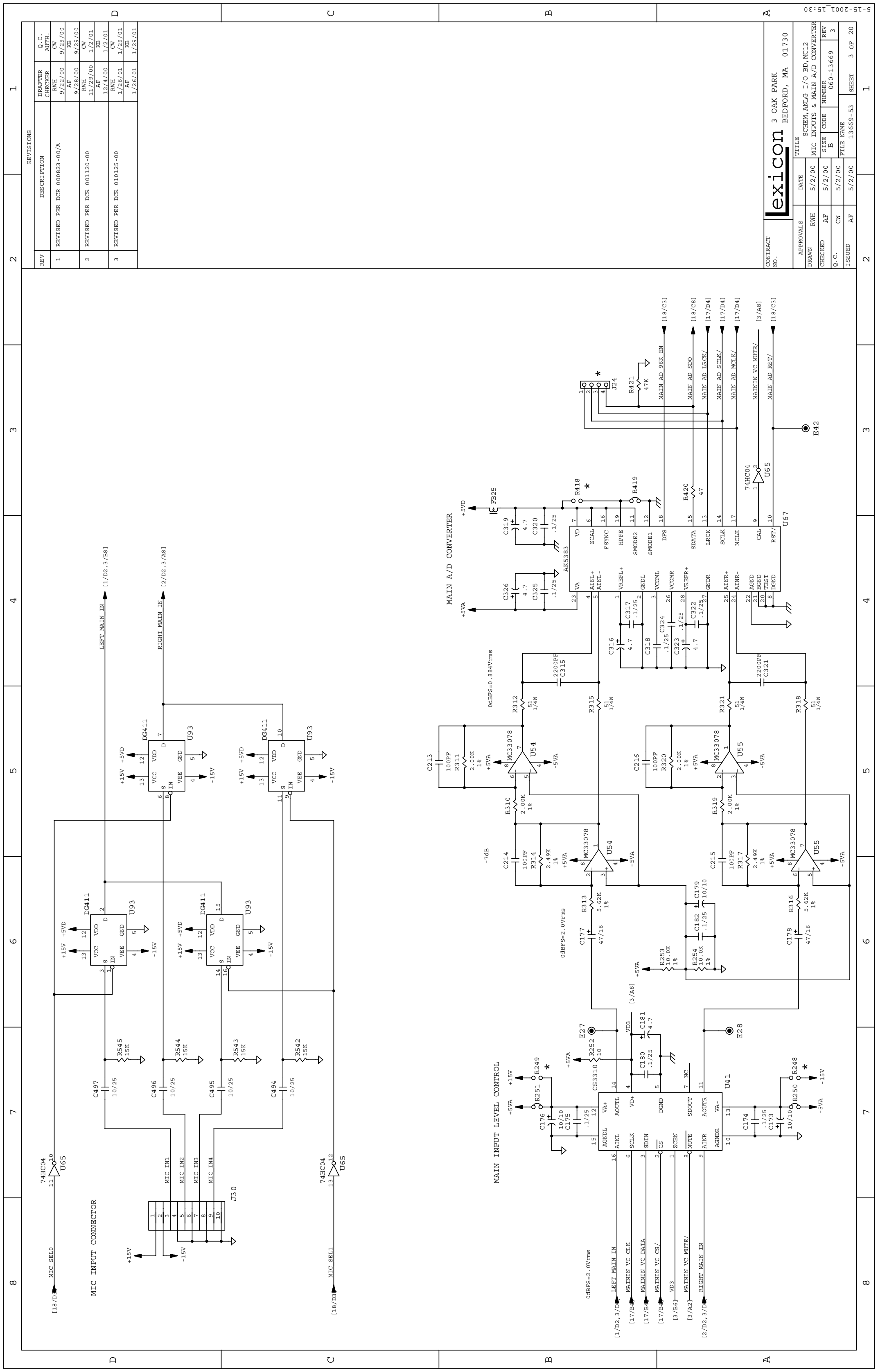
Your Notes:


LEFT ANALOG INPUTS
MAIN SOURCE SELECT
RECORD SOURCE SELECT
ZONE2 SOURCE SELECT
LEFT MAIN IN
LEFT DIR IN
LEFT REC IN
LEFT ZON2 IN
CNTR DIR IN
LSUR DIR IN
REVISIONS
NOTES
© 2001 Lexicon, Inc.
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12
LEFT ANALOG INPUT MUXES
060-13669
SHEET 1 OF 20

Your Notes:

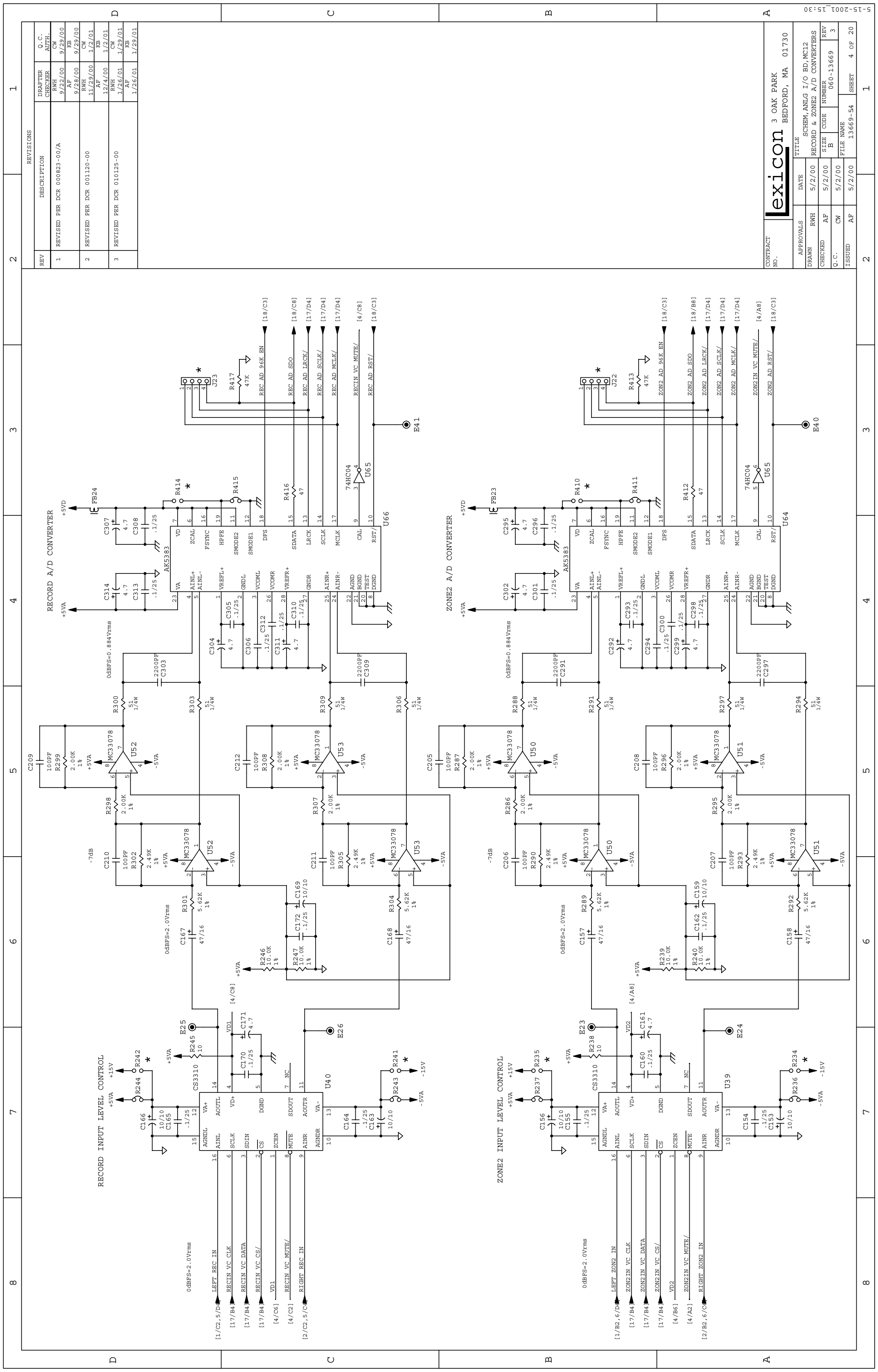

RIGHT ANALOG INPUTS
MAIN SOURCE SELECT
RECORD SOURCE SELECT
ZONE2 SOURCE SELECT
REVISIONS
REVISED PER DCR 000823-00/A
REVISED PER DCR 001120-00
REVISED PER DCR 010125-00
lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12
RIGHT ANALOG INPUT MUXES
060-13669
13669-S2
SHEET 2 OF 20
5-15-2001_15:30

Your Notes:

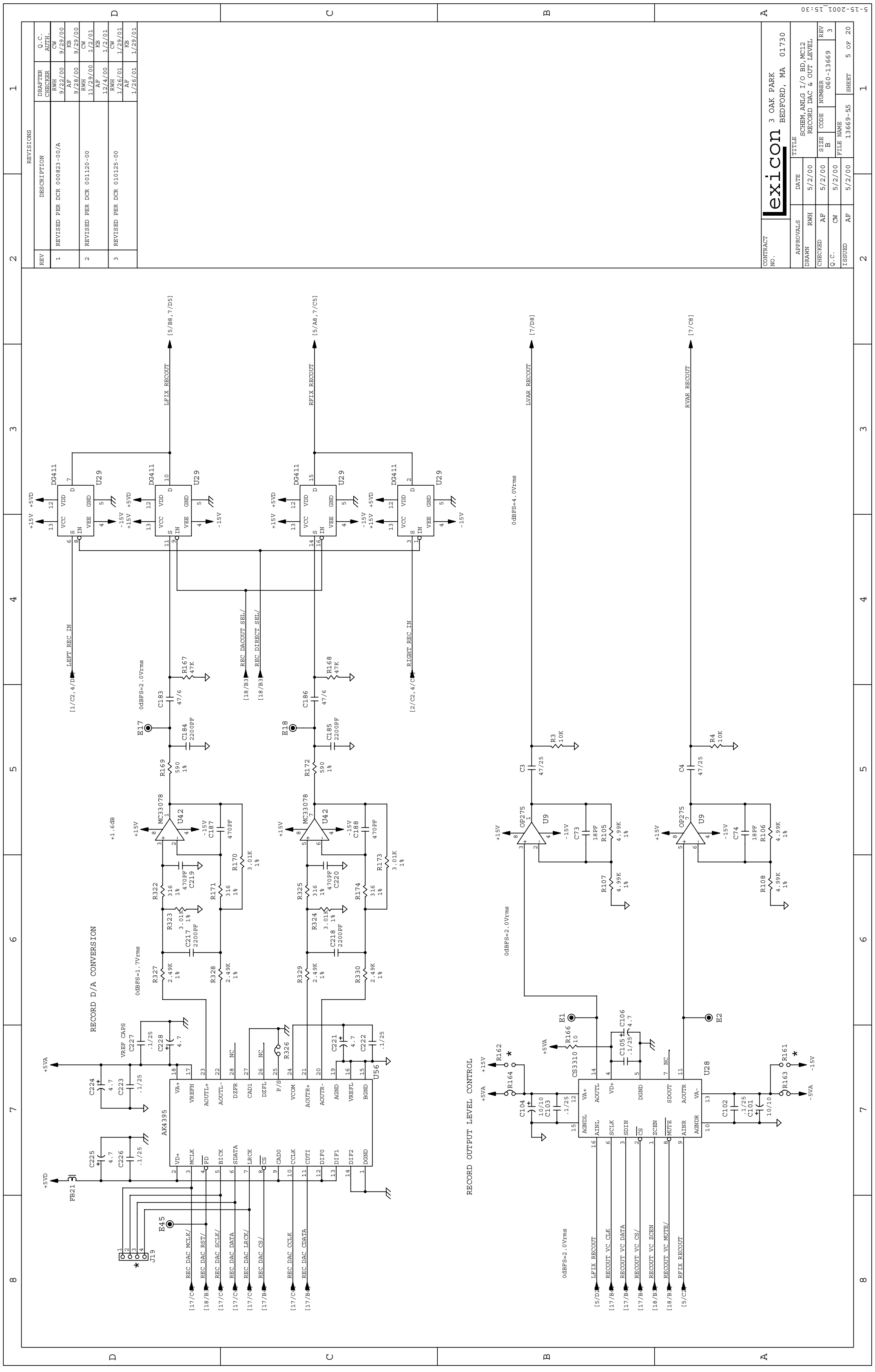


MIC INPUT CONNECTOR
MAIN INPUT LEVEL CONTROL
MAIN A/D CONVERTER
REVISIONS
REV | DESCRIPTION | DRAFTER CHECKER | Q.C. AUTH.
1 | REVISED PER DCR 000823-00/A | RWH 9/22/00 AF 9/28/00 | CW 9/29/00 KB 9/29/00
2 | REVISED PER DCR 001120-00 | RWH 11/29/00 AF 12/4/00 | CW 1/2/01 KB 1/2/01
3 | REVISED PER DCR 010125-00 | RWH 1/26/01 AF 1/26/01 | CW 1/29/01 KB 1/29/01
lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE SCHEM,ANLG I/O BD,MC12 MIC INPUTS & MAIN A/D CONVERTER
DRAWN RWH 5/2/00
CHECKED AF 5/2/00
Q.C. CW 5/2/00
ISSUED AF 5/2/00
SIZE B
NUMBER 060-13669
REV 3
FILE NAME 13669-53
SHEET 3 OF 20
5-15-2001_15:30

Your Notes:

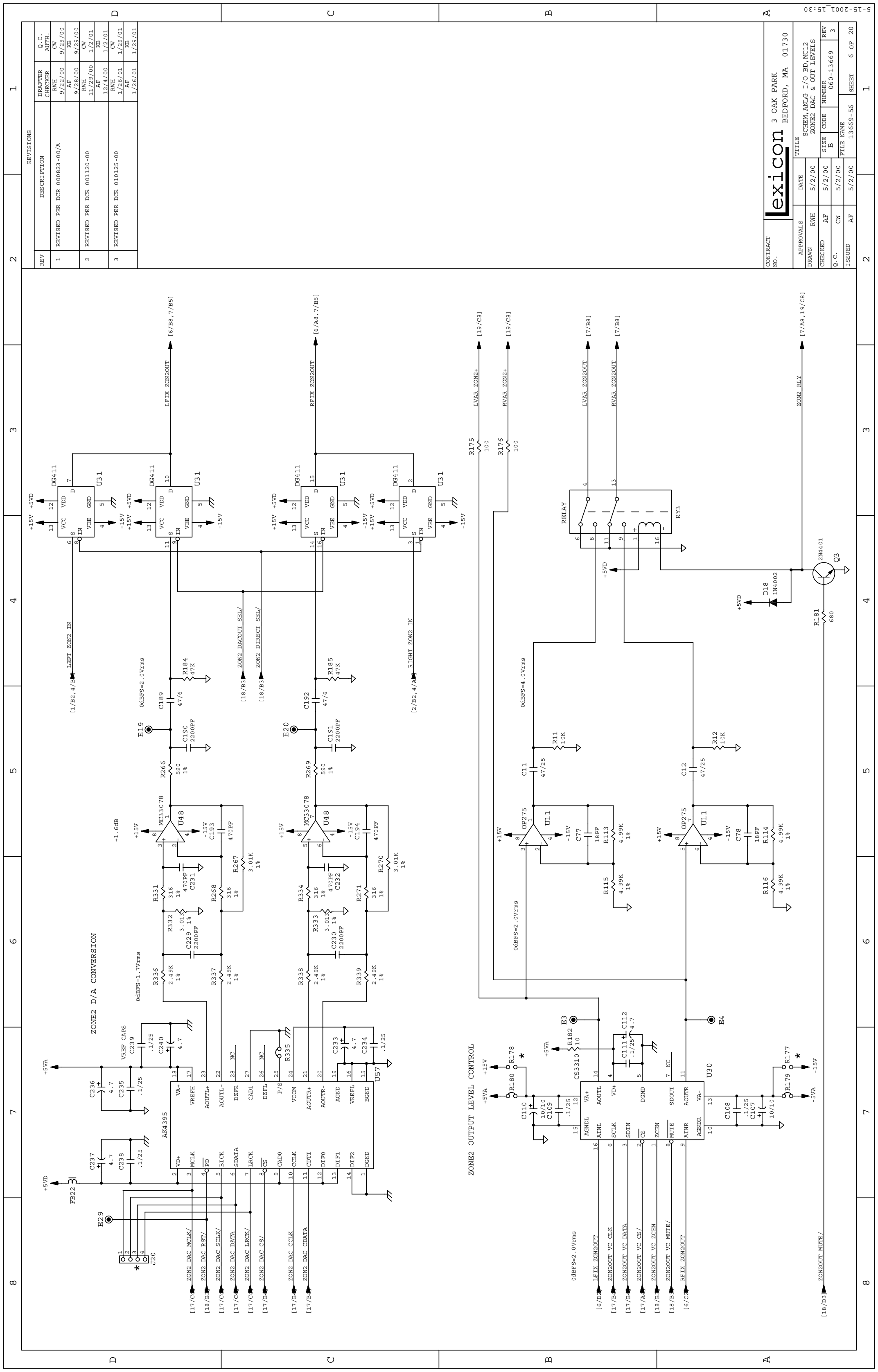

RECORD A/D CONVERTER
ZONE2 A/D CONVERTER
RECORD INPUT LEVEL CONTROL
ZONE2 INPUT LEVEL CONTROL
REVISIONS
REVISED PER DCR 000823-00/A
REVISED PER DCR 001120-00
REVISED PER DCR 010125-00
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12
RECORD & ZONE2 A/D CONVERTERS
060-13669
13669-54
SHEET 4 OF 20
5-15-2001_15:30

Your Notes:

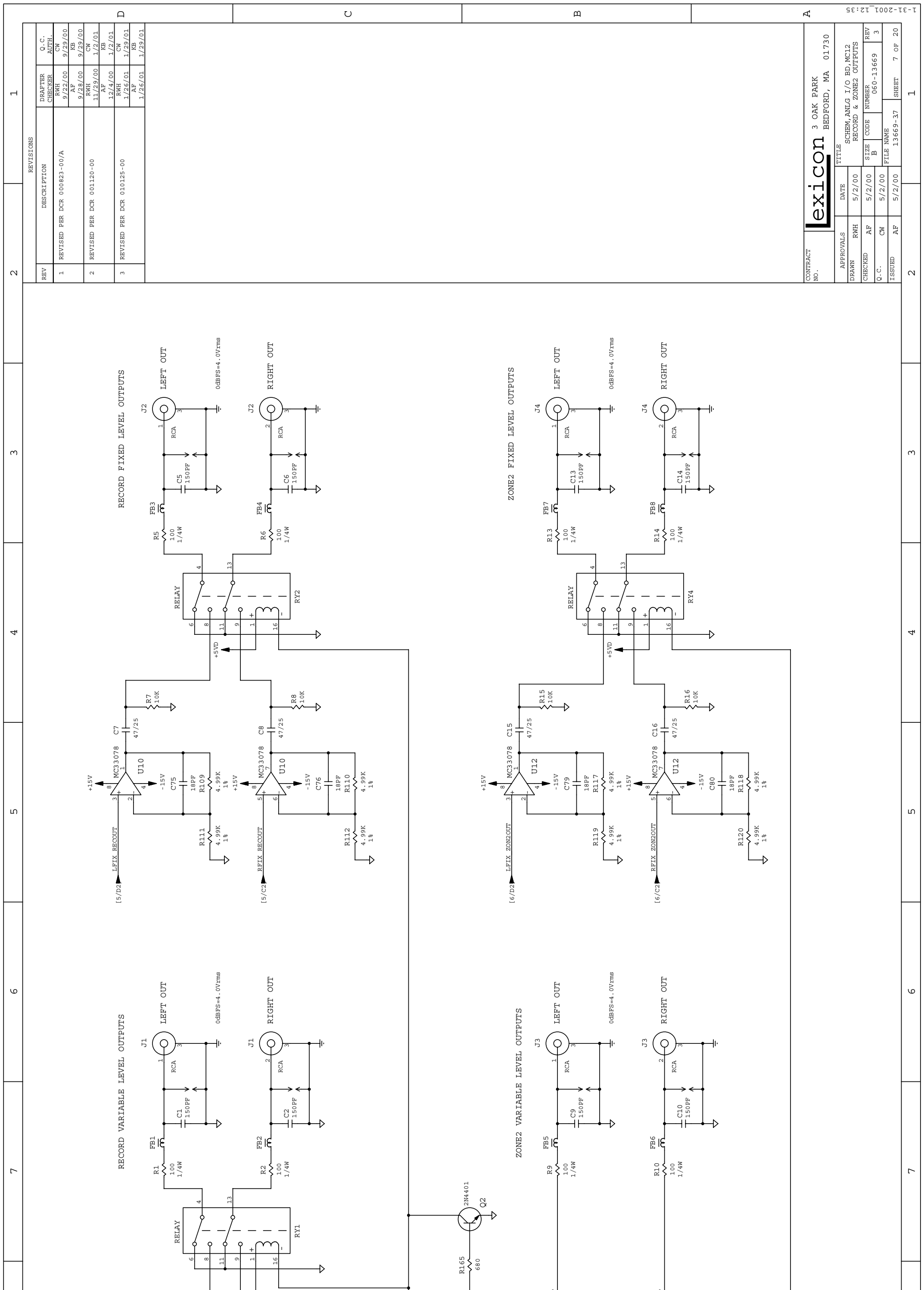


RECORD D/A CONVERSION
RECORD OUTPUT LEVEL CONTROL
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12 RECORD DAC & OUT LEVEL
060-13669
13669-55
SHEET 5 OF 20

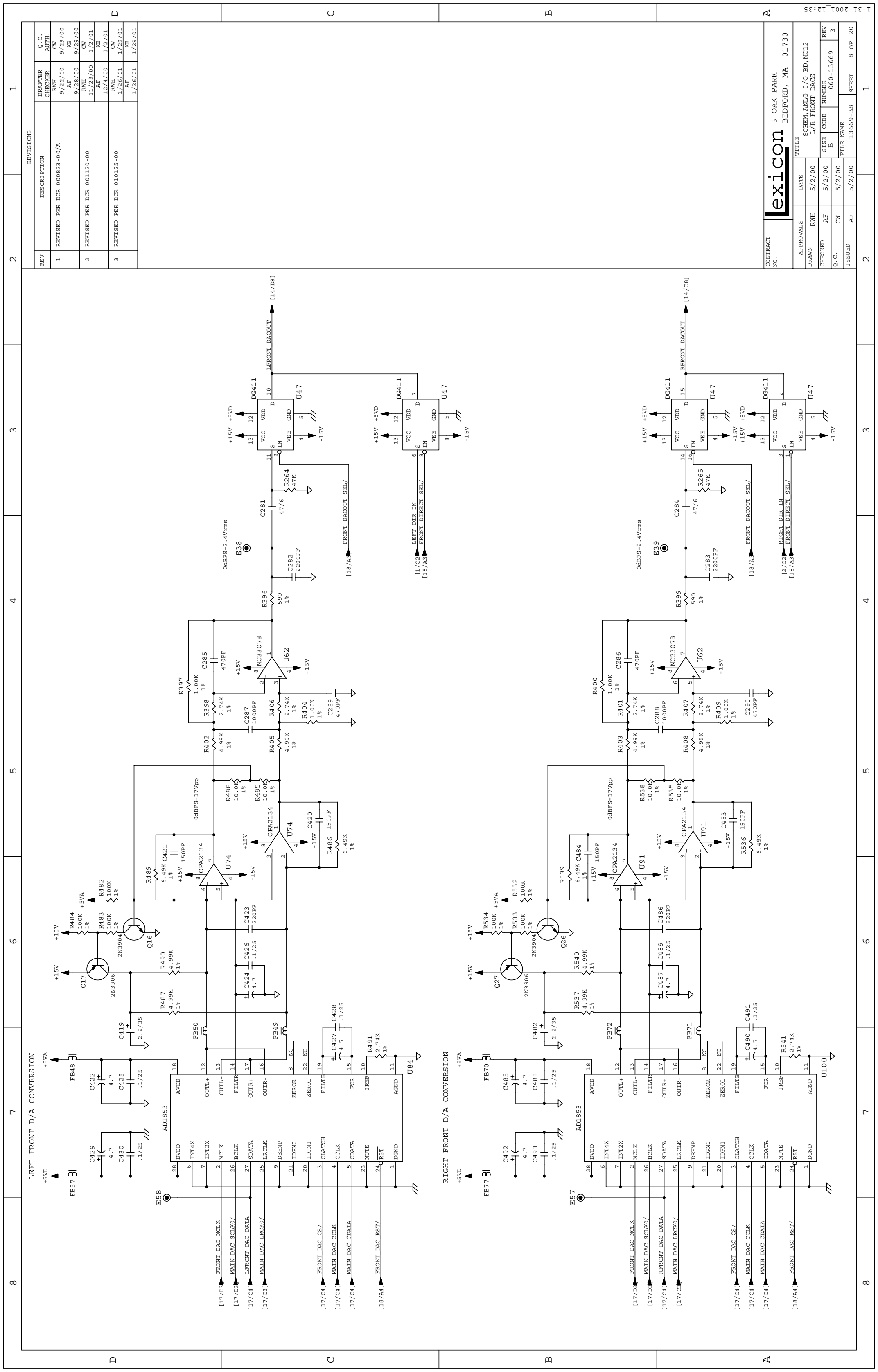
Your Notes:


ZONE2 D/A CONVERSION
ZONE2 OUTPUT LEVEL CONTROL
REVISIONS
REVISED PER DCR 000823-00/A
REVISED PER DCR 001120-00
REVISED PER DCR 010125-00
lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12
ZONE2 DAC & OUT LEVELS
060-13669
13669-56
6 OF 20
5-15-2001_15:30

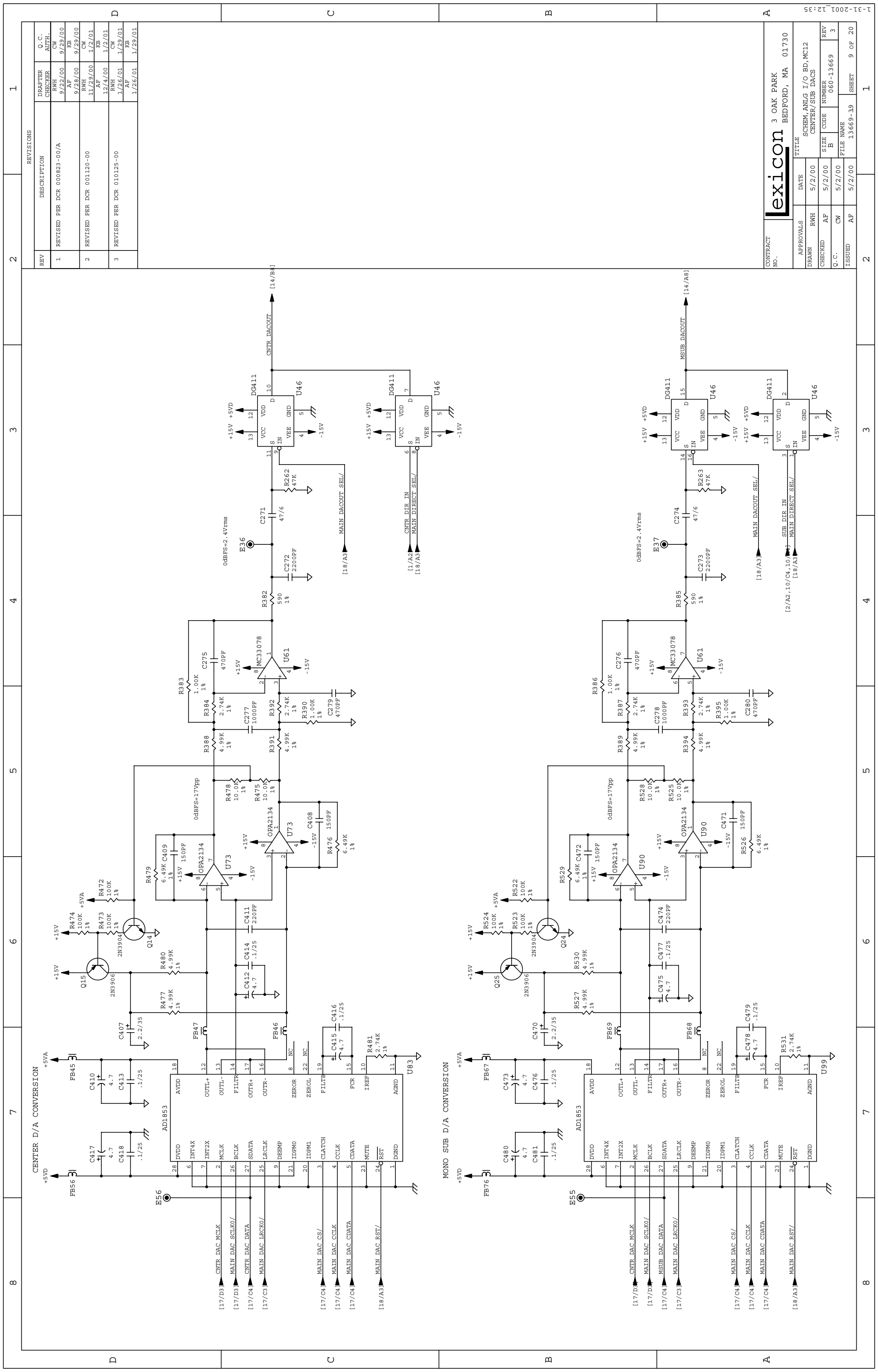
Your Notes:


REVISIONS
REV
DESCRIPTION
DRAFTER CHECKER
Q.C. AUTH.
1 REVISED PER DCR 000823-00/A
2 REVISED PER DCR 001120-00
3 REVISED PER DCR 010125-00
RECORD FIXED LEVEL OUTPUTS
RECORD VARIABLE LEVEL OUTPUTS
ZONE2 FIXED LEVEL OUTPUTS
ZONE2 VARIABLE LEVEL OUTPUTS
LEFT OUT
RIGHT OUT
0dBFS=4.0Vrms
RCA
RELAY
MC33078
2N4401
1N4002
LFIX_RECOUT
RFIX_RECOUT
LFIX_ZON2OUT
RFIX_ZON2OUT
LVAR_RECOUT
RVAR_RECOUT
RECOUT_MUTE/
LVAR_ZON2OUT
RVAR_ZON2OUT
ZON2_RLY
lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE SCHEM,ANLG I/O BD,MC12 RECORD & ZONE2 OUTPUTS
NUMBER 060-13669
REV 3
SIZE B
FILE NAME 13669-37
SHEET 7 OF 20
APPROVALS
DRAWN RWH 5/2/00
CHECKED AP 5/2/00
Q.C. CW 5/2/00
ISSUED AP 5/2/00
1-31-2001_12:35

Your Notes:

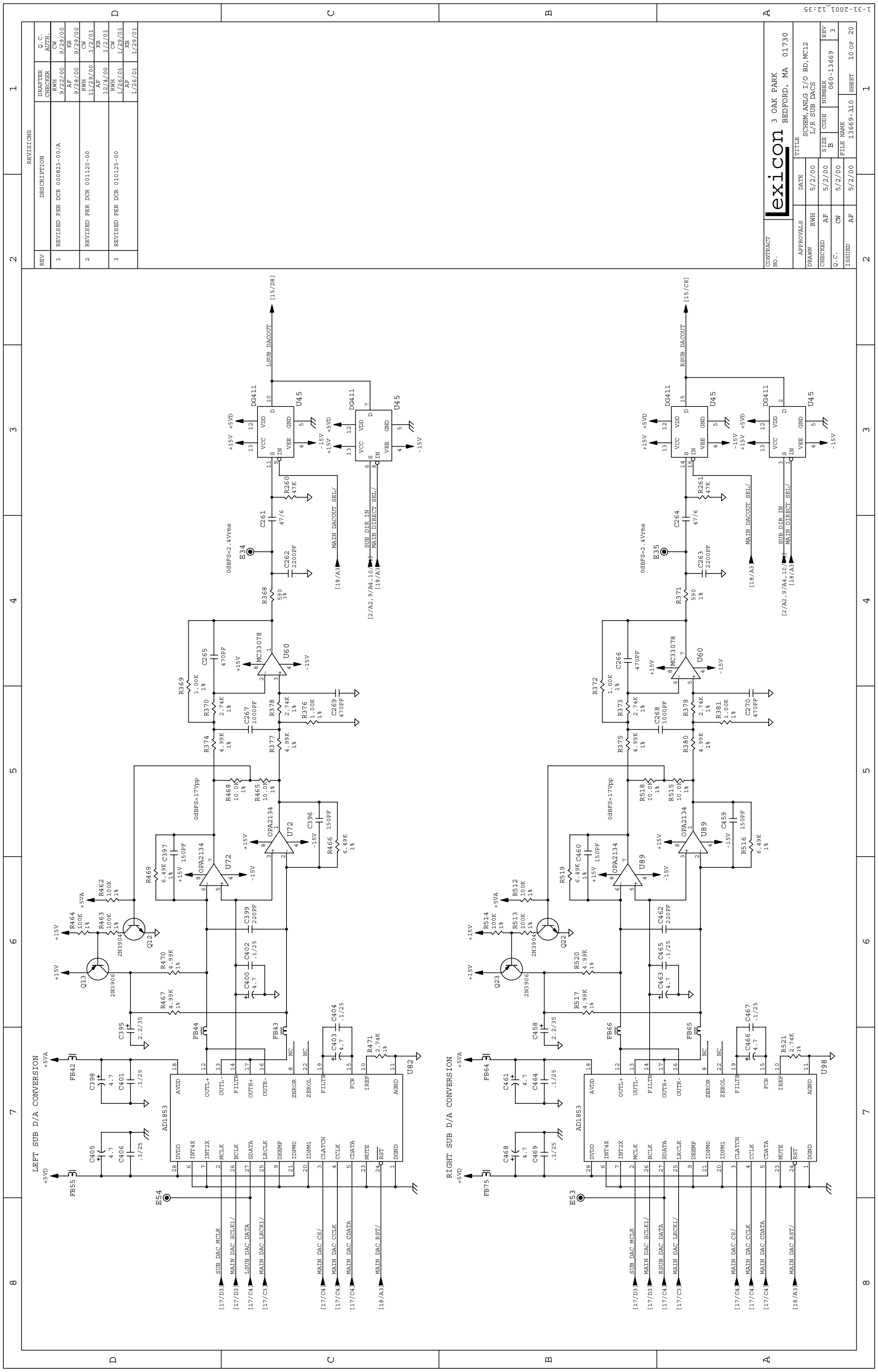

LEFT FRONT D/A CONVERSION
RIGHT FRONT D/A CONVERSION
REVISIONS
REV | DESCRIPTION | DRAFTER CHECKER | Q.C. AUTH.
1 REVISED PER DCR 000823-00/A
2 REVISED PER DCR 001120-00
3 REVISED PER DCR 010125-00
lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE SCHEM,ANLG I/O BD,MC12 L/R FRONT DACS
SIZE B
NUMBER 060-13669
REV 3
FILE NAME 13669-38
SHEET 8 OF 20
APPROVALS DATE
DRAWN RWH 5/2/00
CHECKED AP 5/2/00
Q.C. CW 5/2/00
ISSUED AP 5/2/00
1-31-2001_12:35

Your Notes:

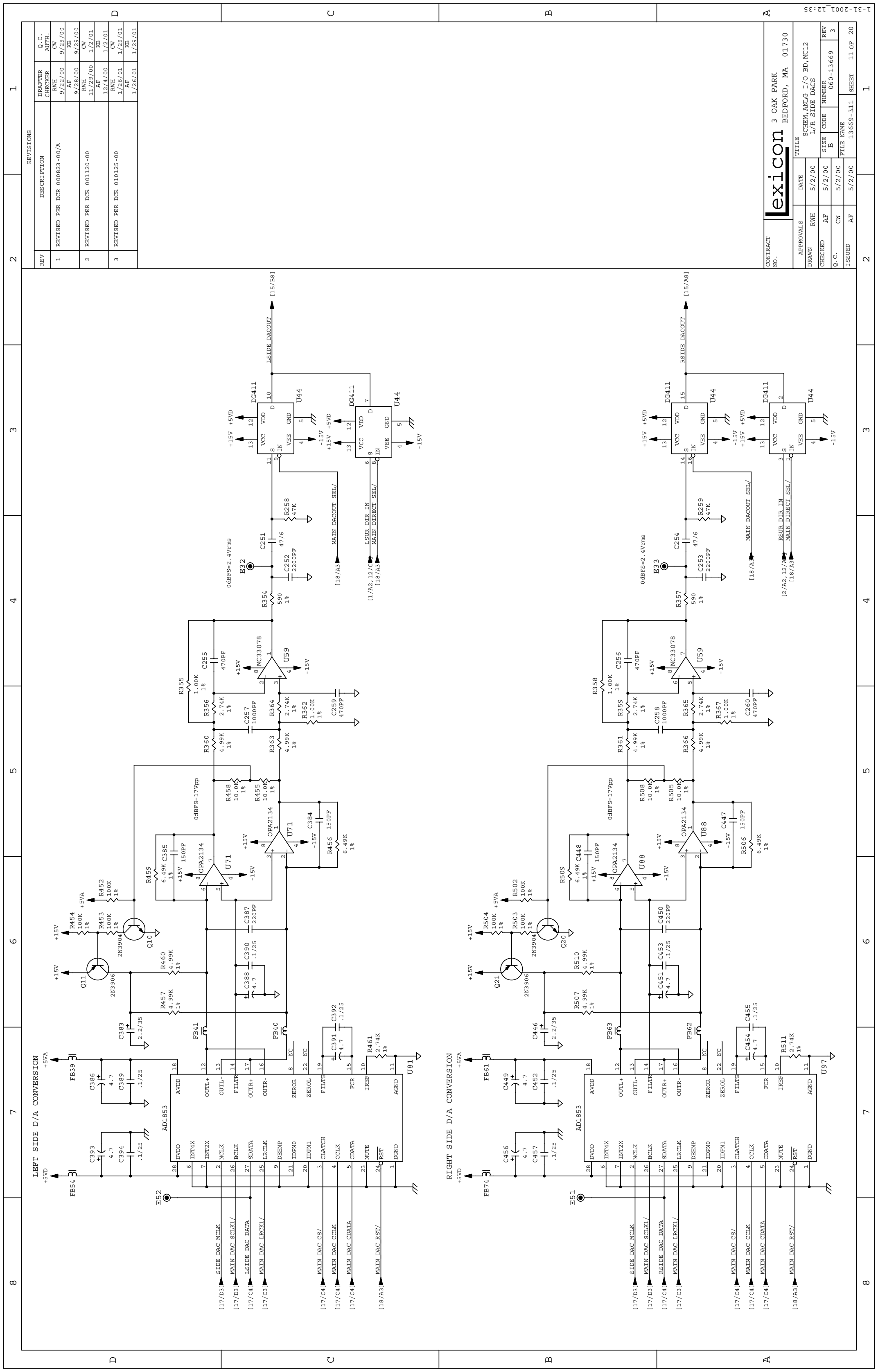


CENTER D/A CONVERSION
MONO SUB D/A CONVERSION
REVISIONS
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12 CENTER/SUB DACS
060-13669
SHEET 9 OF 20

Your Notes:

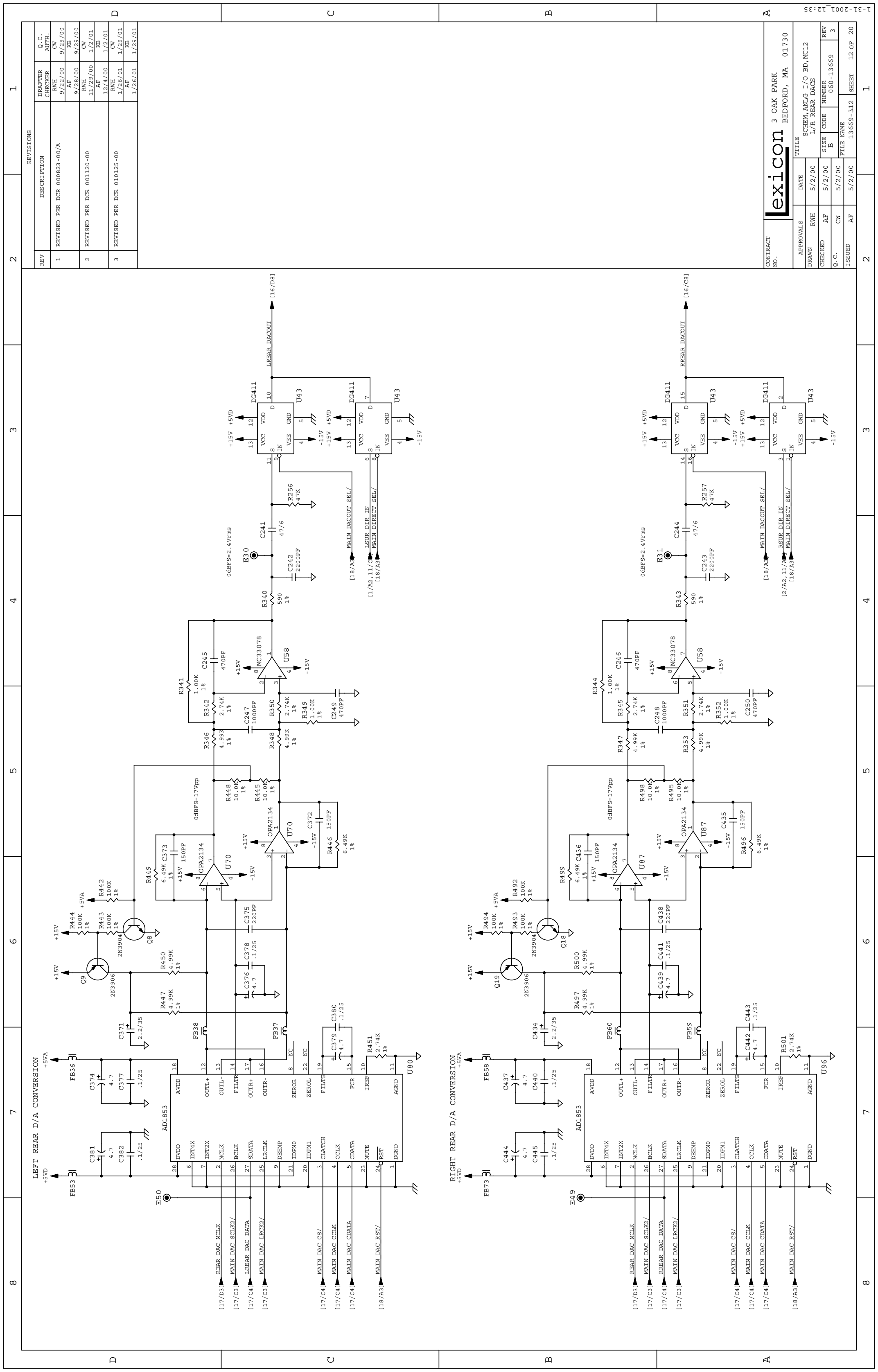

LEFT SUB D/A CONVERSION
RIGHT SUB D/A CONVERSION
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12 L/R SUB DACS
060-13669
13669-310
REVISIONS
REVISED PER DCR 000823-00/A
REVISED PER DCR 001120-00
REVISED PER DCR 010125-00

Your Notes:

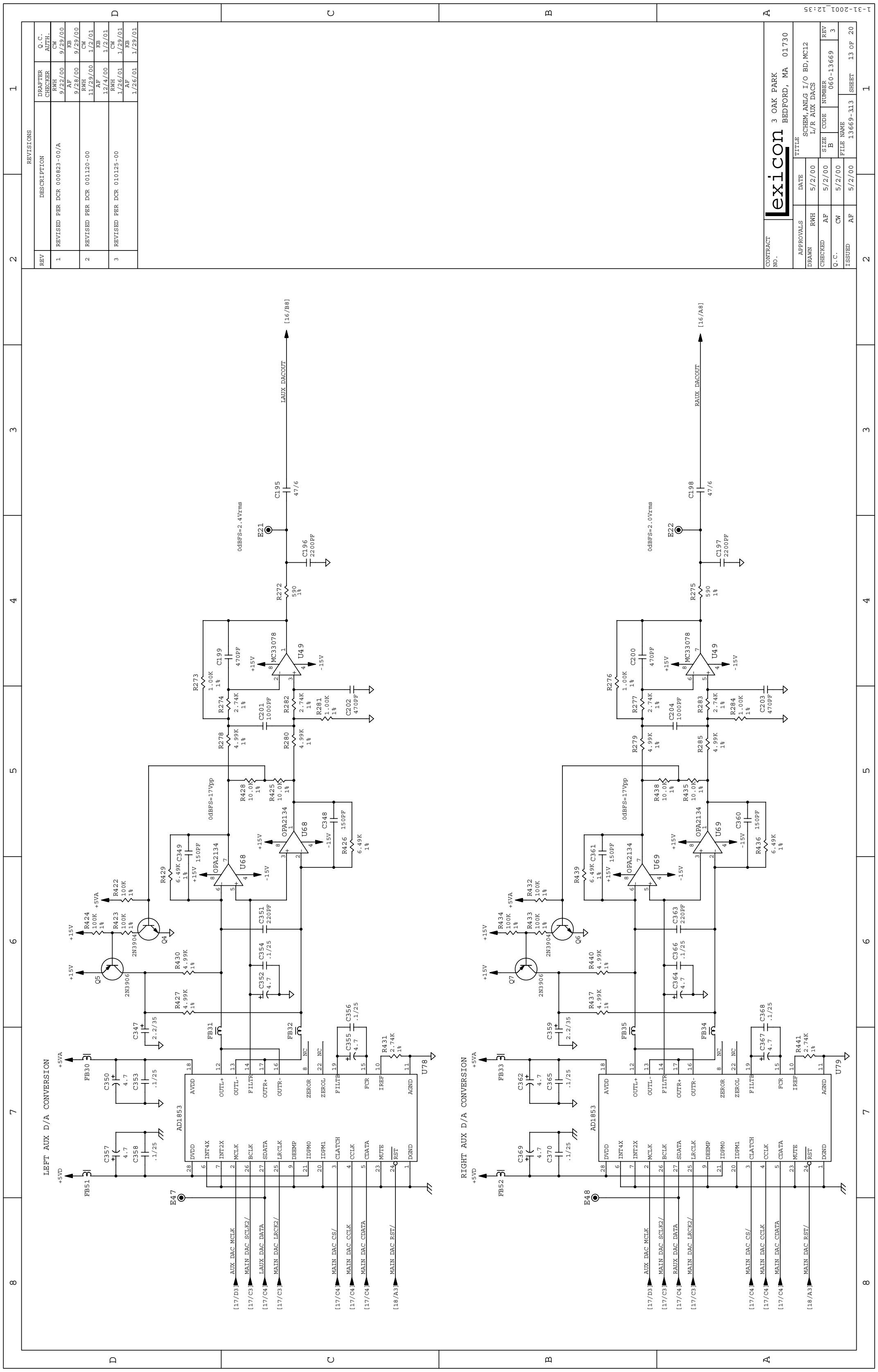


LEFT SIDE D/A CONVERSION
RIGHT SIDE D/A CONVERSION
AD1853
OPA2134
MC33078
DG411
LSIDE DACOUT
RSIDE DACOUT
REVISIONS
REVISED PER DCR 000823-00/A
REVISED PER DCR 001120-00
REVISED PER DCR 010125-00
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12
L/R SIDE DACS
060-13669
13669-311
11 OF 20

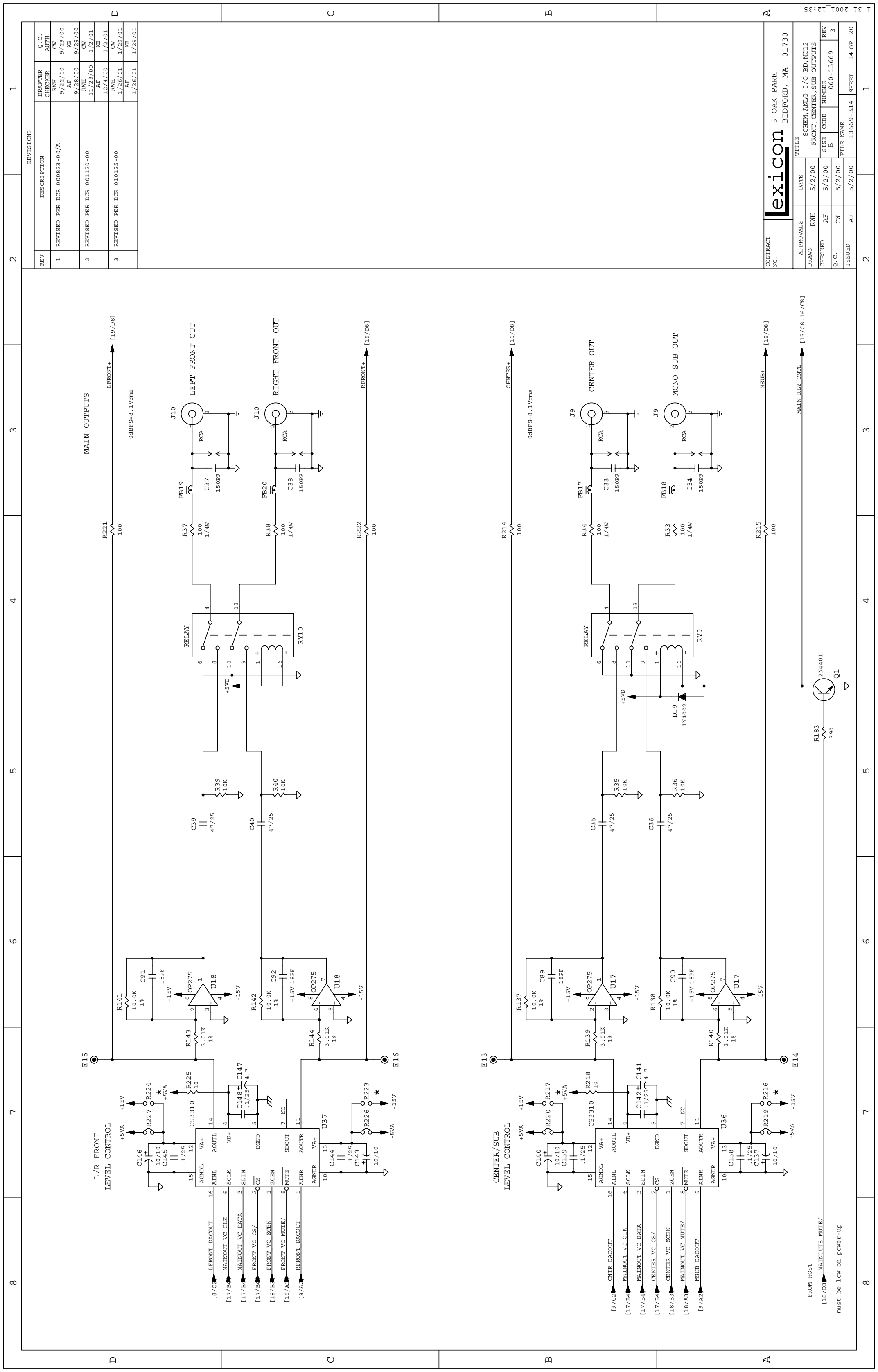
Your Notes:


LEFT REAR D/A CONVERSION
RIGHT REAR D/A CONVERSION
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12
L/R REAR DACS
060-13669
13669-312
12 OF 20

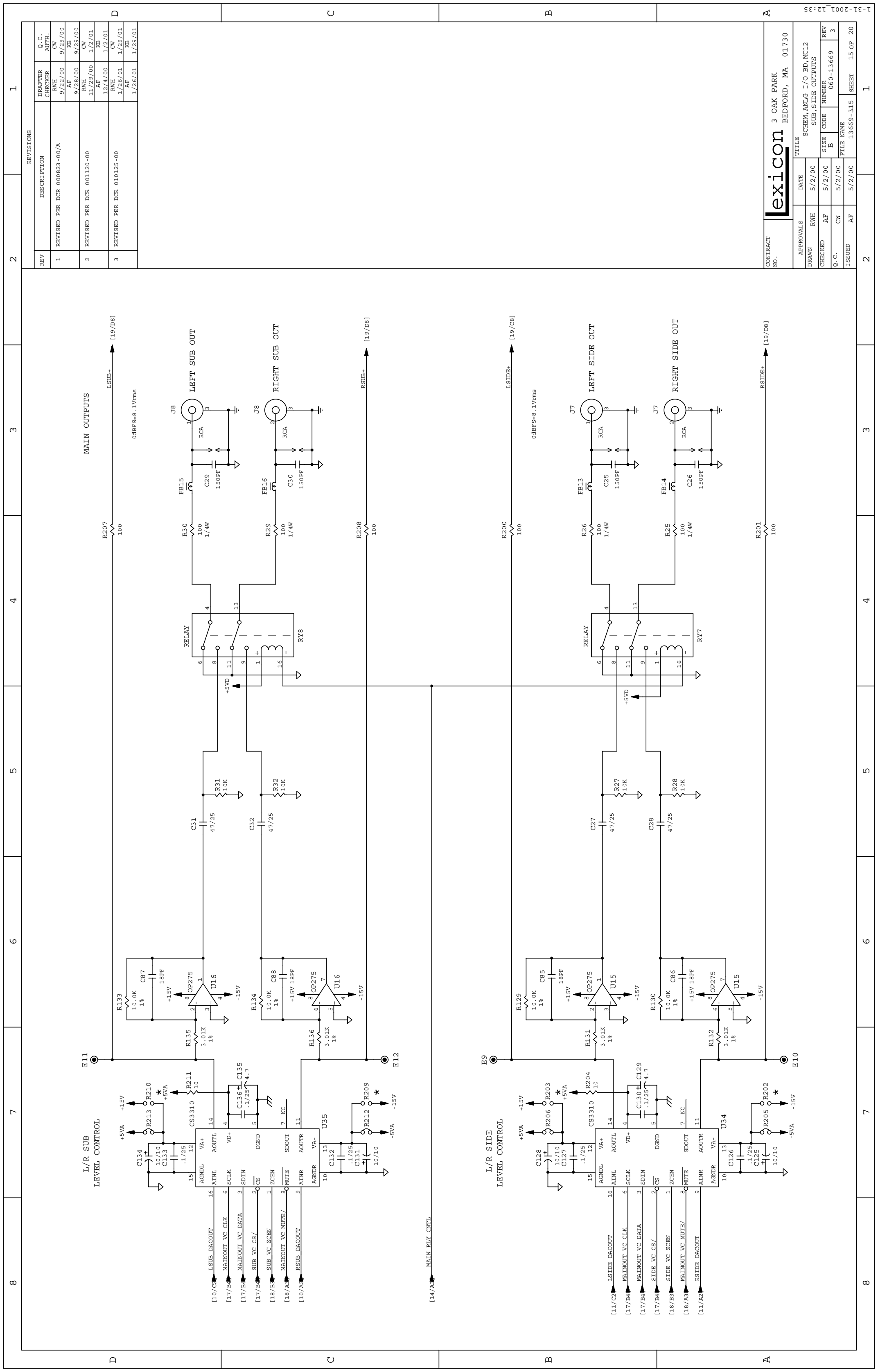
Your Notes:


LEFT AUX D/A CONVERSION
RIGHT AUX D/A CONVERSION
REVISIONS
REVISED PER DCR 000823-00/A
REVISED PER DCR 001120-00
REVISED PER DCR 010125-00
lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12
L/R AUX DACS
060-13669
13669-313
SHEET 13 OF 20

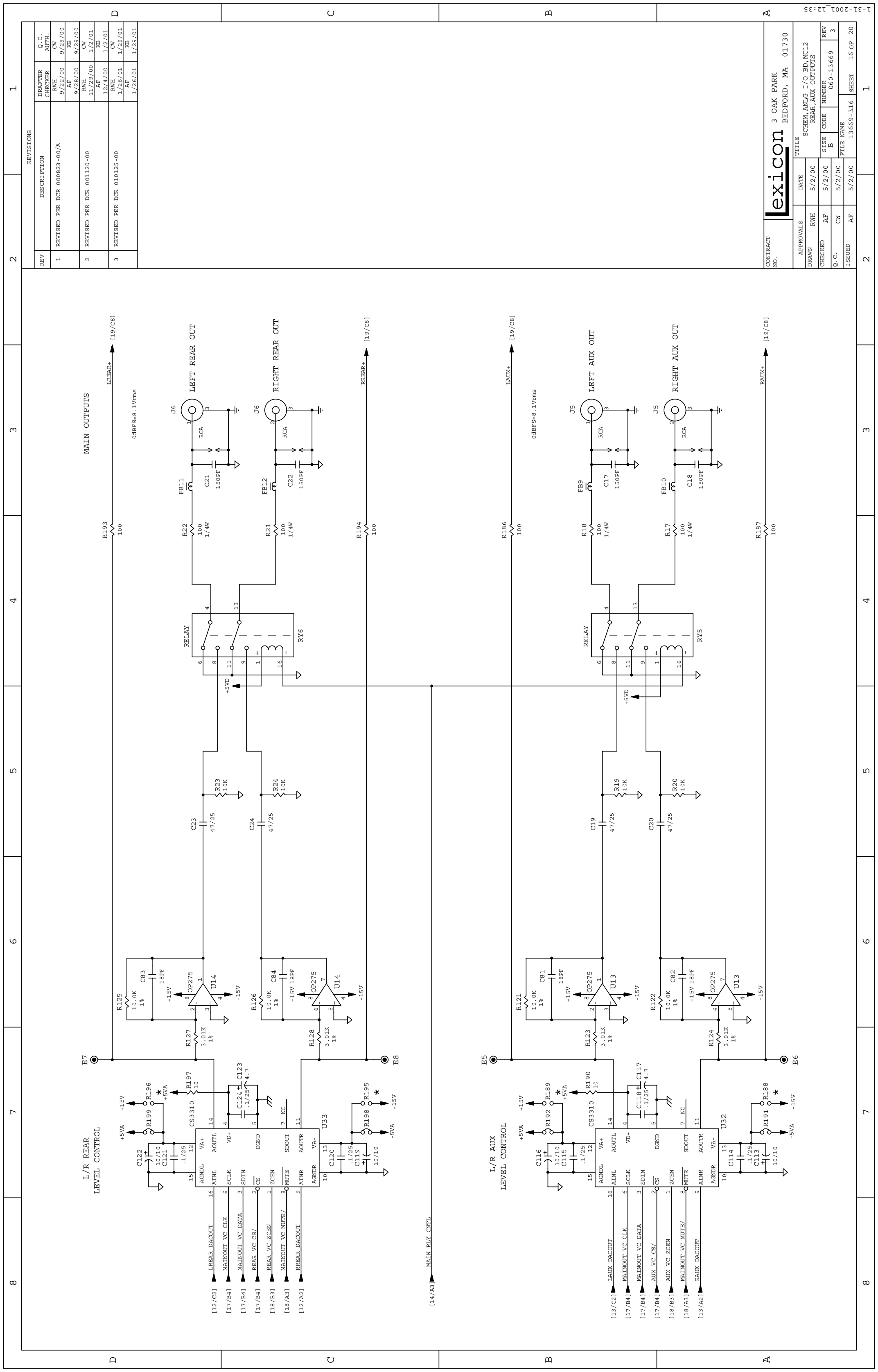
Your Notes:


lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12 FRONT,CENTER,SUB OUTPUTS
060-13669
MAIN OUTPUTS
LEFT FRONT OUT
RIGHT FRONT OUT
CENTER OUT
MONO SUB OUT
L/R FRONT LEVEL CONTROL
CENTER/SUB LEVEL CONTROL

Your Notes:

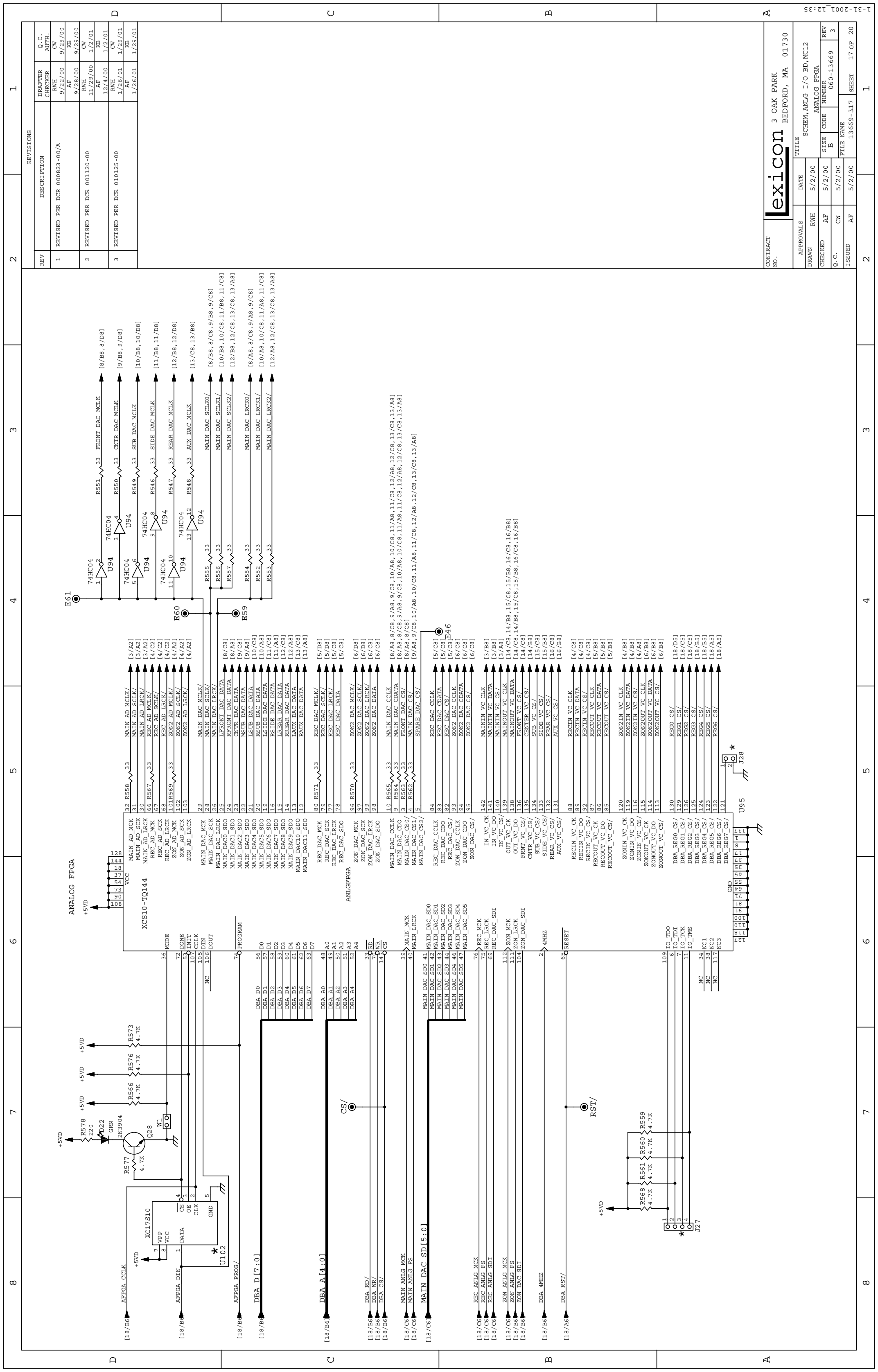

MAIN OUTPUTS
LEFT SUB OUT
RIGHT SUB OUT
LEFT SIDE OUT
RIGHT SIDE OUT
L/R SUB LEVEL CONTROL
L/R SIDE LEVEL CONTROL
REVISIONS
REVISED PER DCR 000823-00/A
REVISED PER DCR 001120-00
REVISED PER DCR 010125-00
lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE SCHEM,ANLG I/O BD,MC12 SUB,SIDE OUTPUTS
SIZE B
NUMBER 060-13669
REV 3
FILE NAME 13669-315
SHEET 15 OF 20

Your Notes:

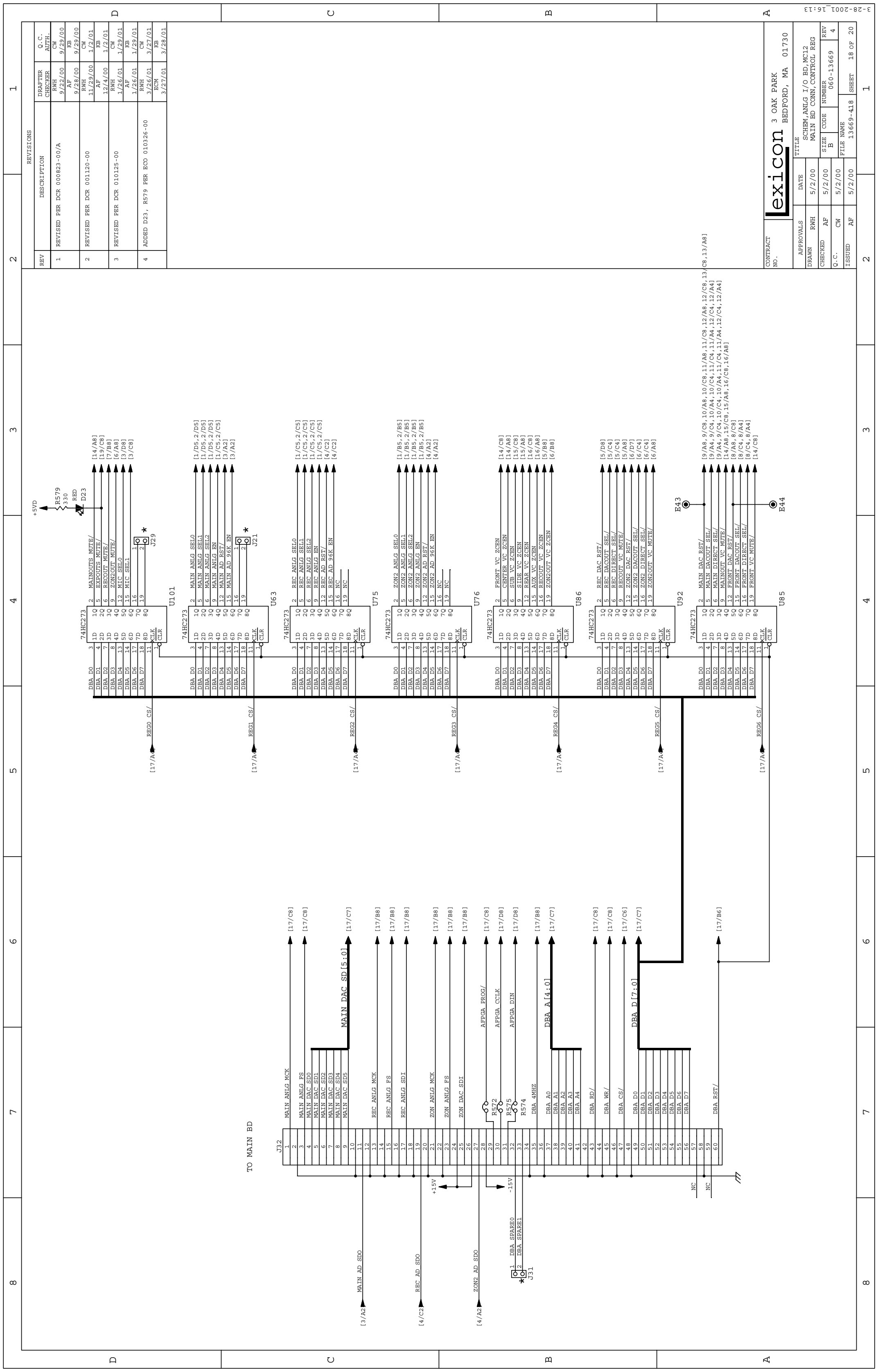


MAIN OUTPUTS
LEFT REAR OUT
RIGHT REAR OUT
LEFT AUX OUT
RIGHT AUX OUT
L/R REAR LEVEL CONTROL
L/R AUX LEVEL CONTROL
REVISIONS
REVISED PER DCR 000823-00/A
REVISED PER DCR 001120-00
REVISED PER DCR 010125-00
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12 REAR,AUX OUTPUTS
060-13669
13669-316
SHEET 16 OF 20

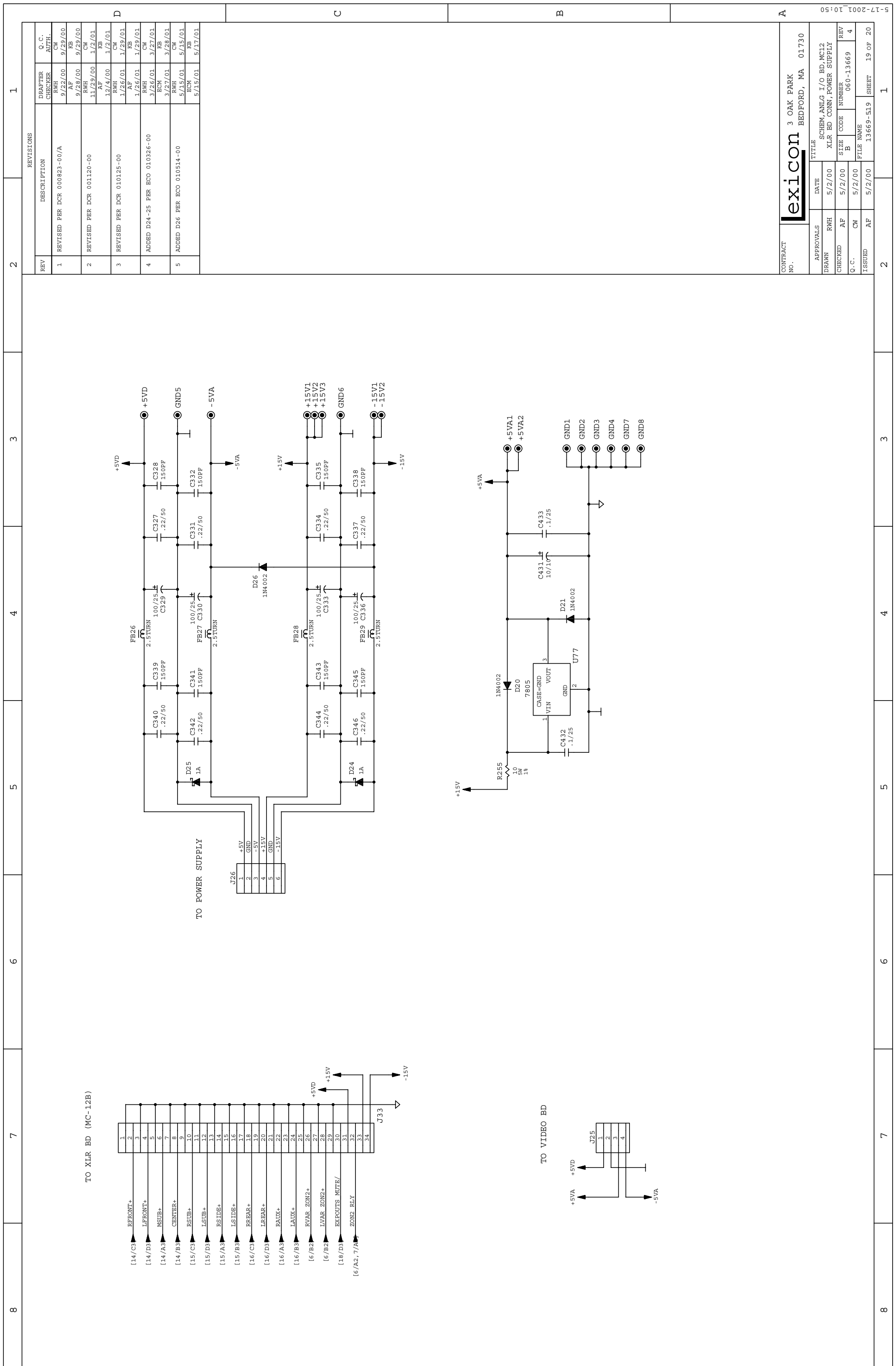
Your Notes:


ANALOG FPGA
XCS10-TQ144
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12
ANALOG FPGA
060-13669
13669-317
SHEET 17 OF 20

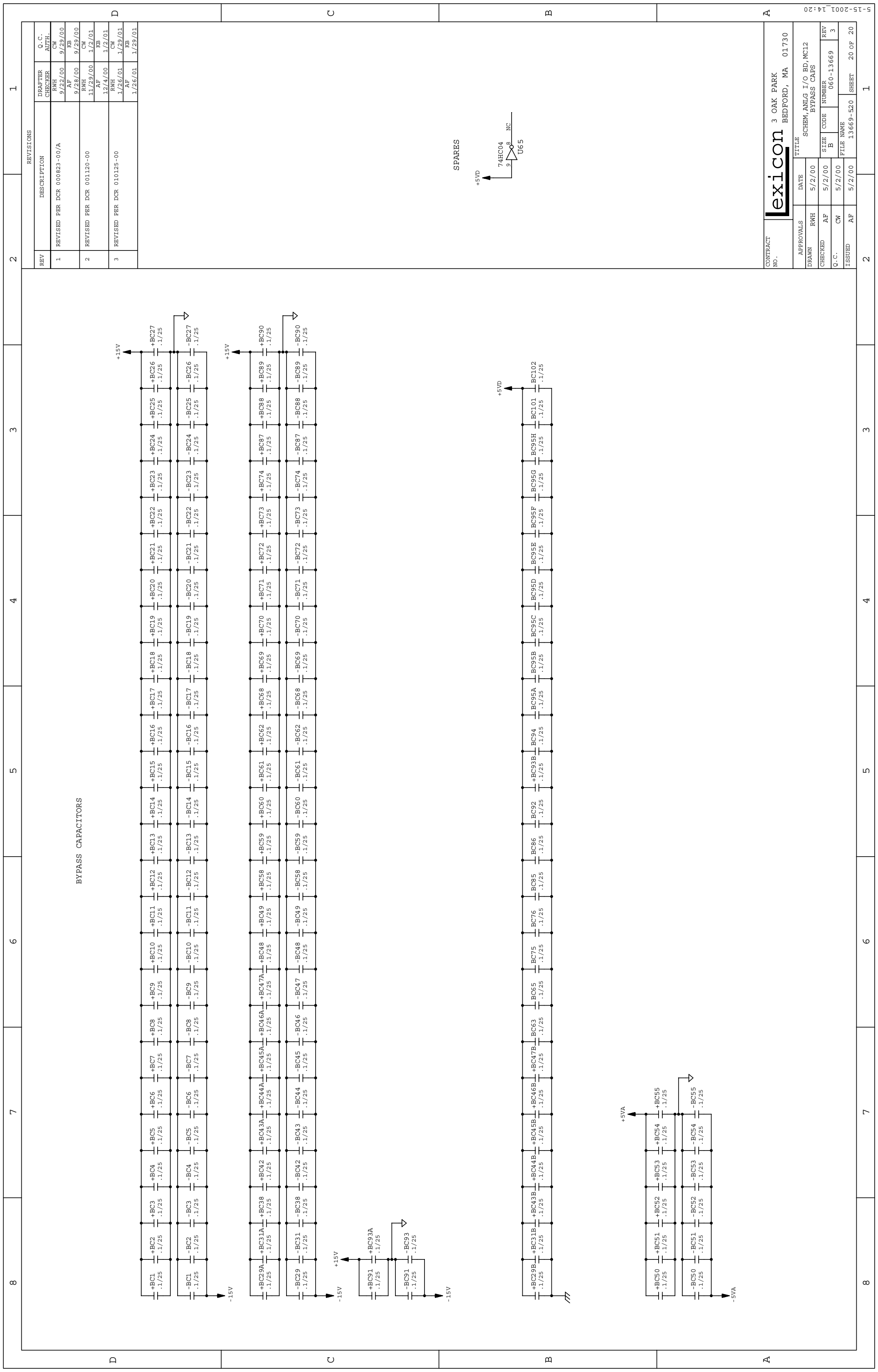
Your Notes:


lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12
MAIN BD CONN,CONTROL REG
060-13669
TO MAIN BD

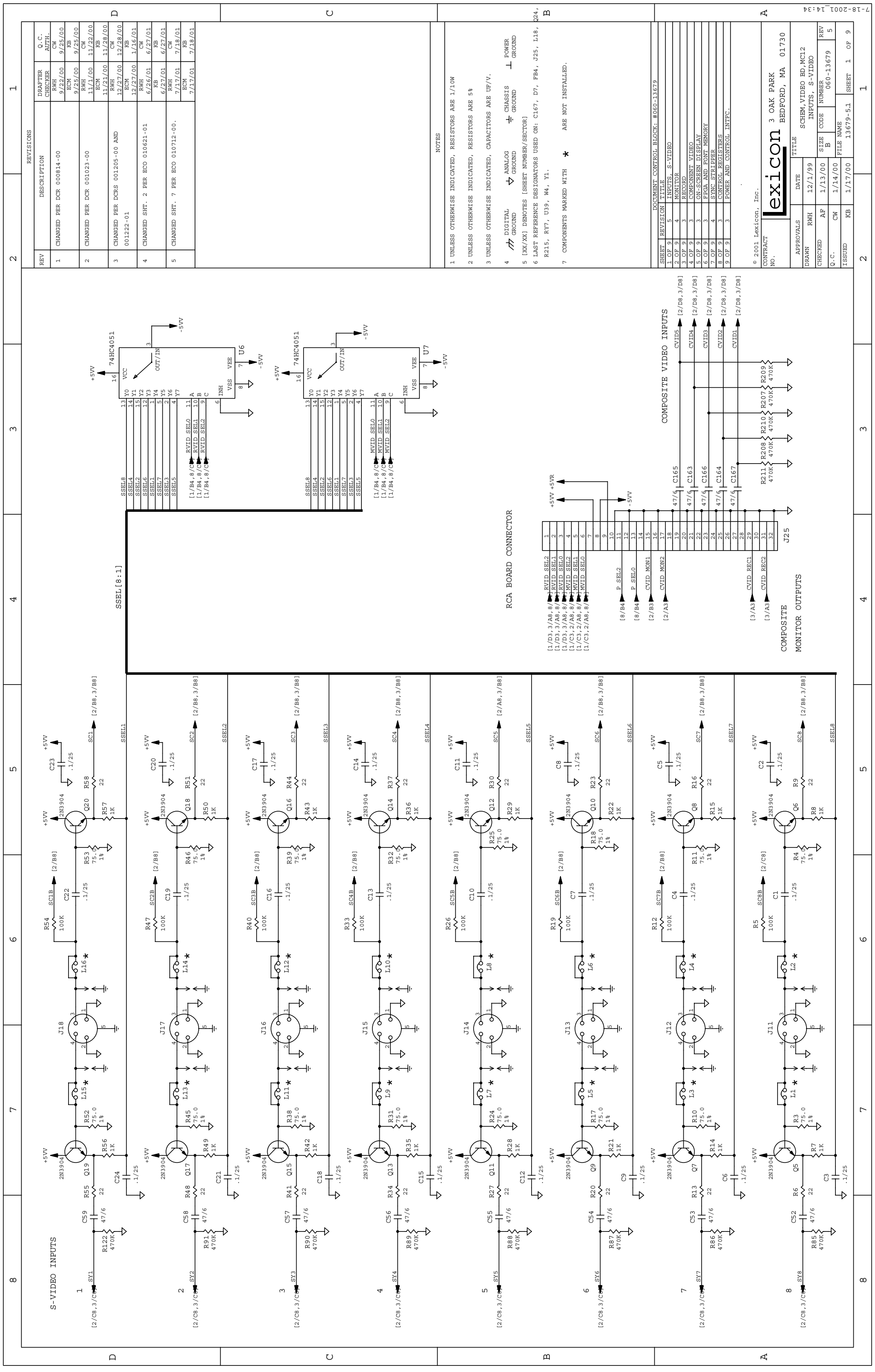
Your Notes:


lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE SCHEM,ANLG I/O BD,MC12 XLR BD CONN,POWER SUPPLY
SIZE B
NUMBER 060-13669
REV 4
FILE NAME 13669-S19
SHEET 19 OF 20
TO POWER SUPPLY
TO XLR BD (MC-12B)
TO VIDEO BD

Your Notes:

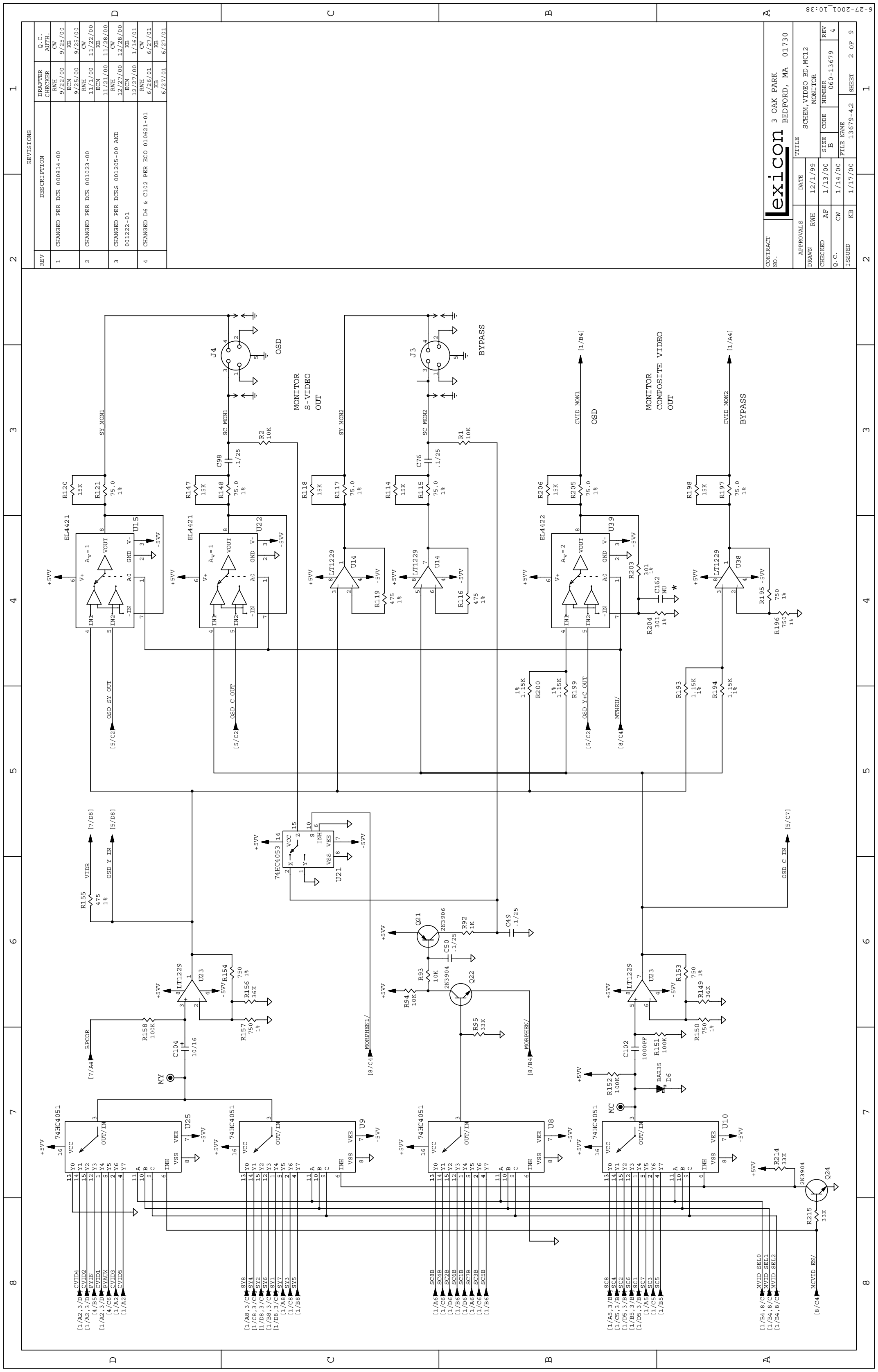

BYPASS CAPACITORS
SPARES
74HC04
U65
lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,ANLG I/O BD,MC12
BYPASS CAPS
060-13669
13669-S20
SHEET 20 OF 20
REVISIONS
REVISED PER DCR 000823-00/A
REVISED PER DCR 001120-00
REVISED PER DCR 010125-00
5-15-2001_14:20

Your Notes:



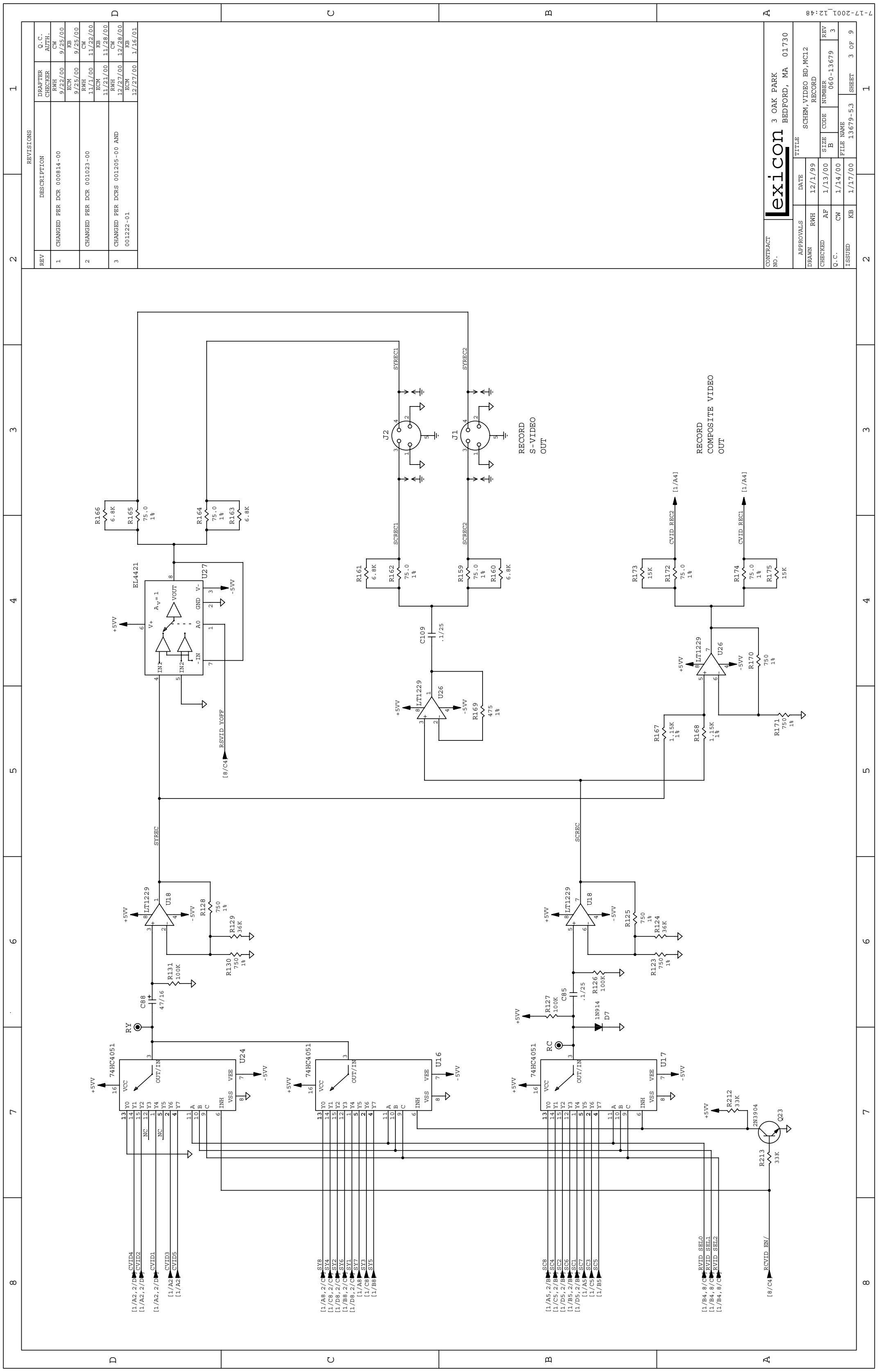
S-VIDEO INPUTS
COMPOSITE VIDEO INPUTS
RCA BOARD CONNECTOR
COMPOSITE MONITOR OUTPUTS
SSEL[8:1]
74HC4051
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,VIDEO BD,MC12 INPUTS, S-VIDEO
060-13679
13679-5.1
SHEET 1 OF 9

Your Notes:

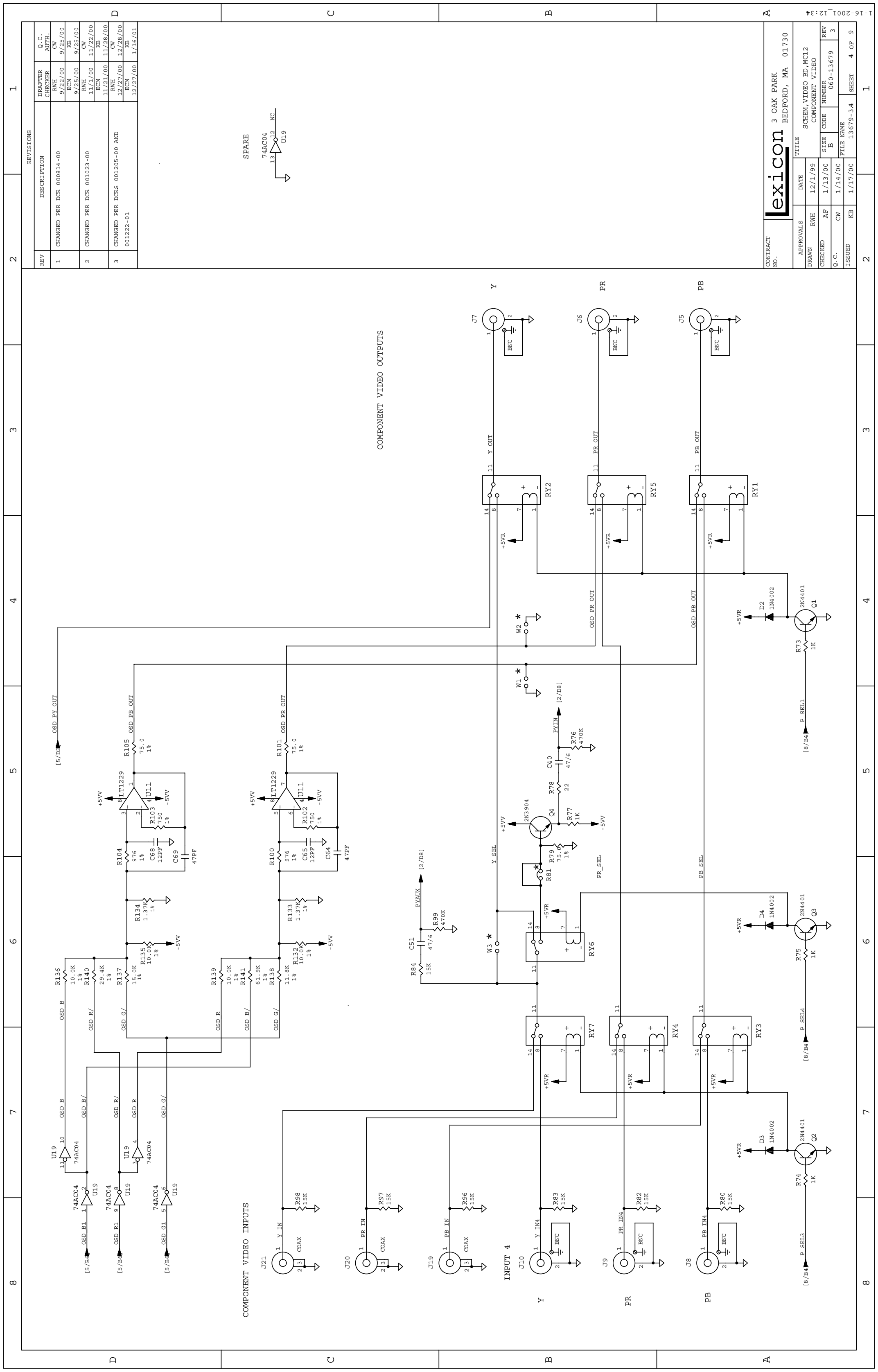


3 OAK PARK
BEDFORD, MA 01730
SCHEM,VIDEO BD,MC12 MONITOR
060-13679
SHEET 2 OF 9
MONITOR S-VIDEO OUT
MONITOR COMPOSITE VIDEO OUT
OSD
BYPASS

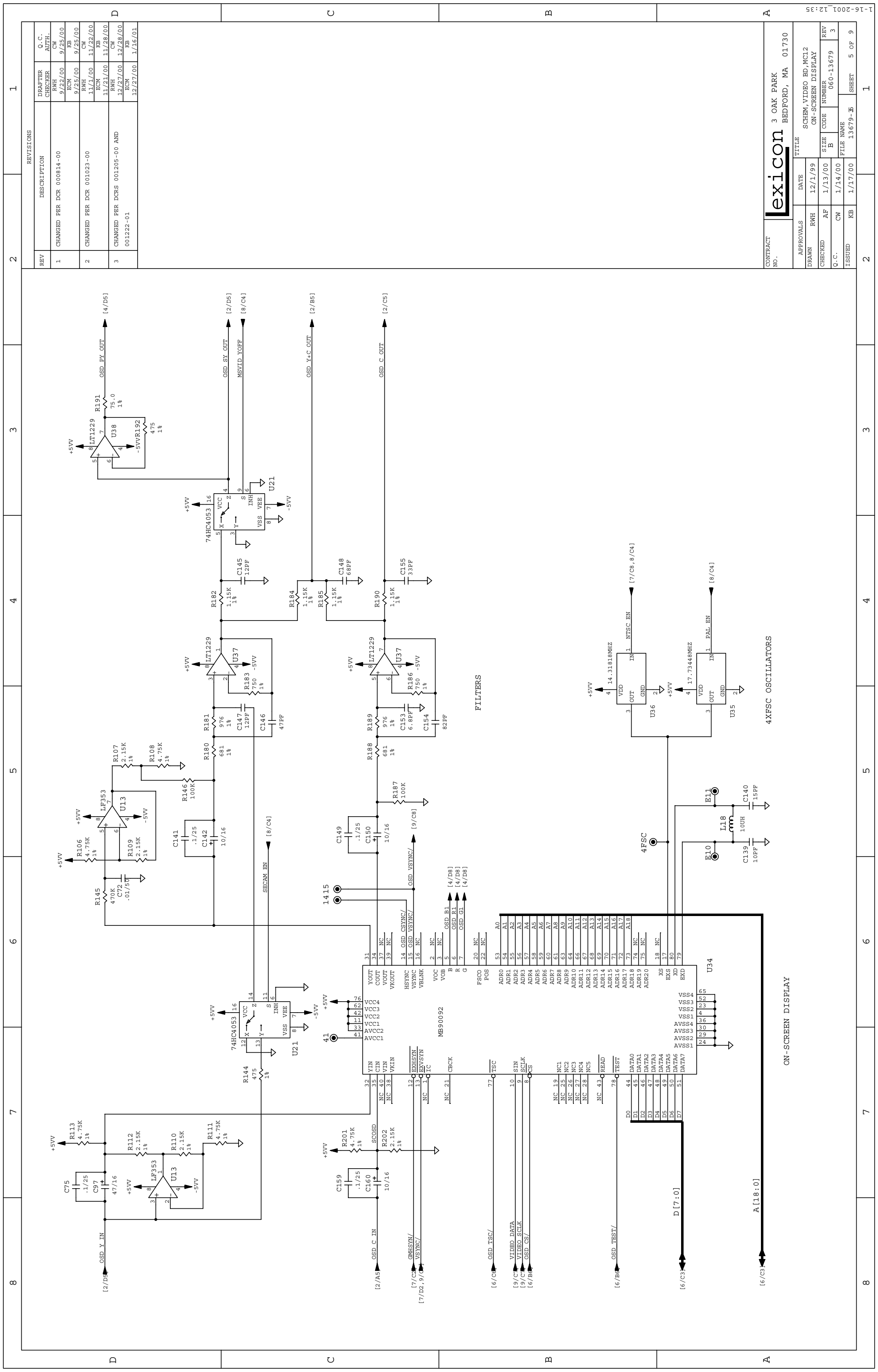
Your Notes:


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,VIDEO BD,MC12
RECORD
060-13679
13679-53
SHEET 3 OF 9
RECORD
S-VIDEO
OUT
RECORD
COMPOSITE VIDEO
OUT

Your Notes:

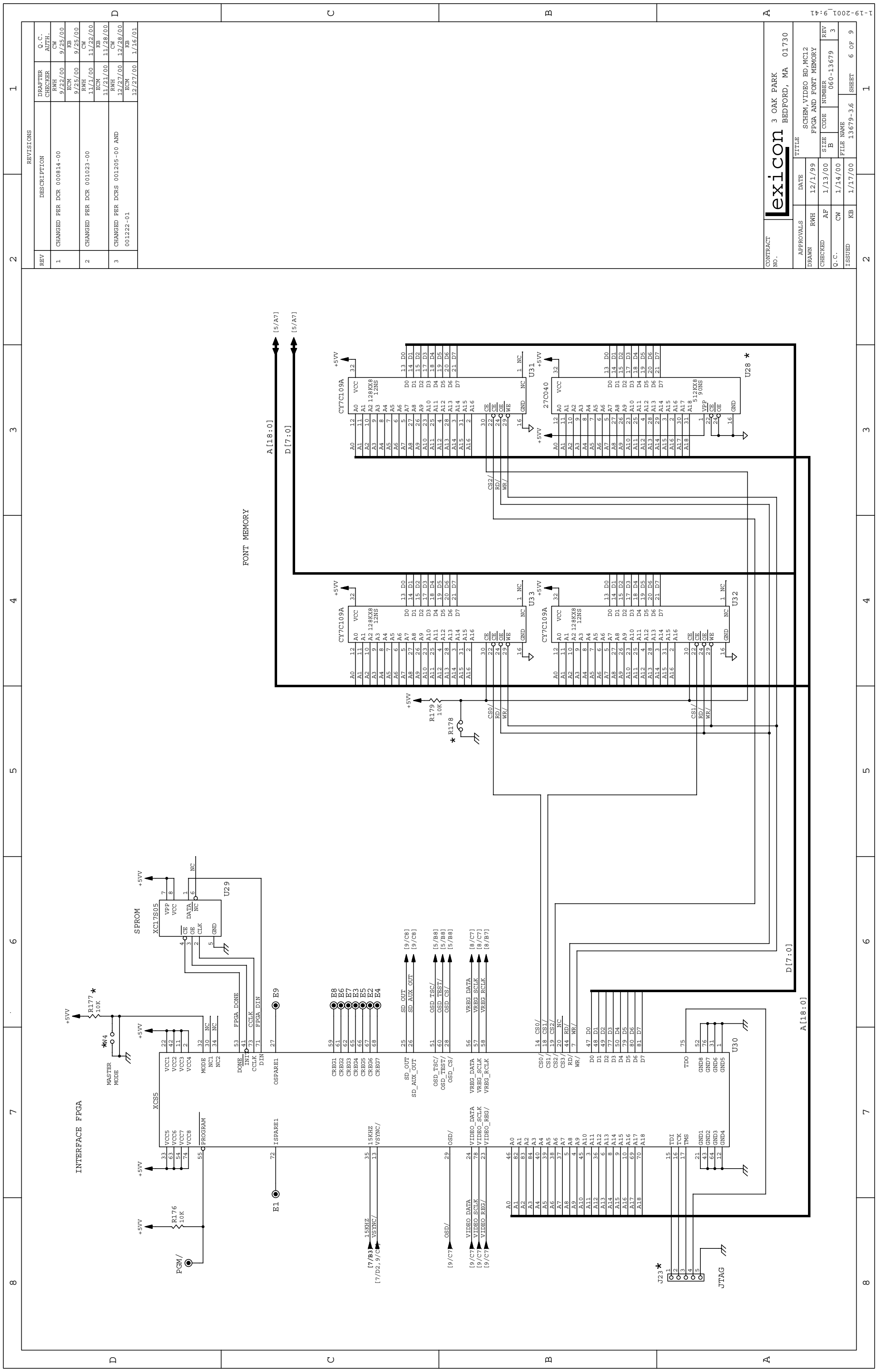

COMPONENT VIDEO OUTPUTS
COMPONENT VIDEO INPUTS
INPUT 4
SPARE
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,VIDEO BD,MC12
COMPONENT VIDEO
060-13679
REV 3
13679-34
SHEET 4 OF 9
1-16-2001_12:34

Your Notes:

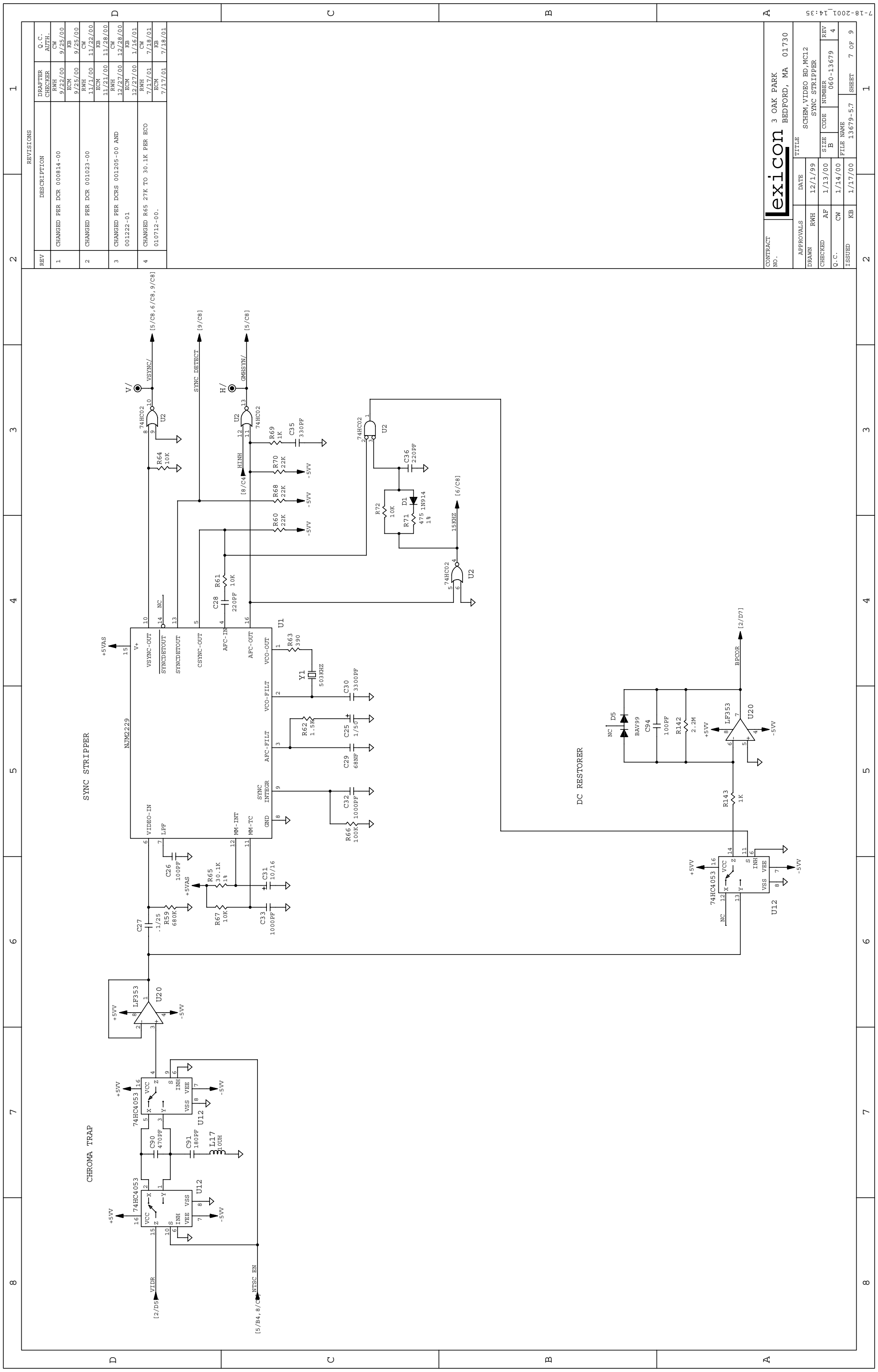


lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,VIDEO BD,MC12 ON-SCREEN DISPLAY
060-13679
FILTERS
4XFSC OSCILLATORS
ON-SCREEN DISPLAY

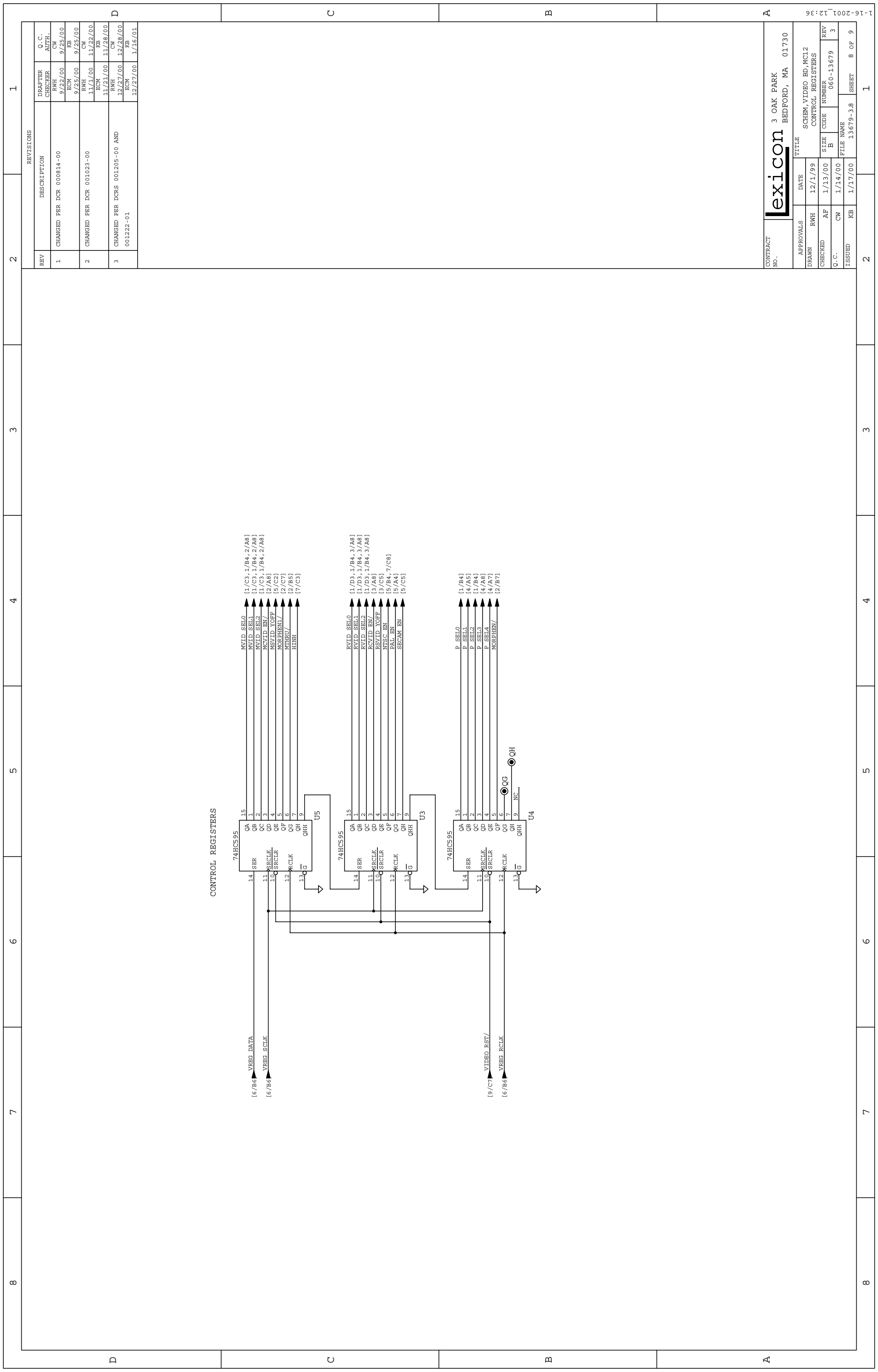
Your Notes:


lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,VIDEO BD,MC12
FPGA AND FONT MEMORY
060-13679
INTERFACE FPGA
FONT MEMORY
SPROM
JTAG

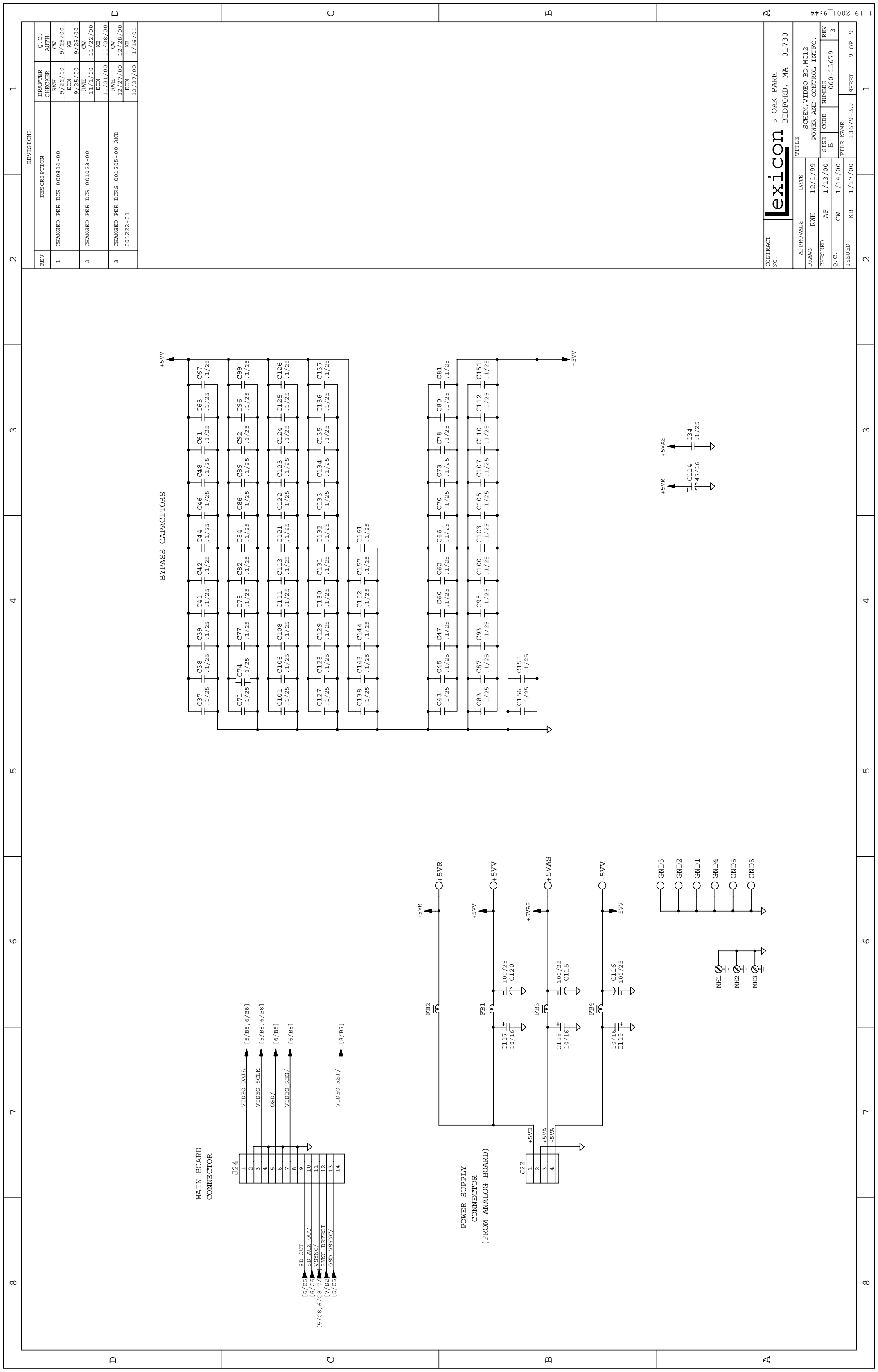
Your Notes:


SYNC STRIPPER
DC RESTORER
CHROMA TRAP
REVISIONS
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,VIDEO BD,MC12
SYNC STRIPPER
060-13679
13679-57
7 OF 9

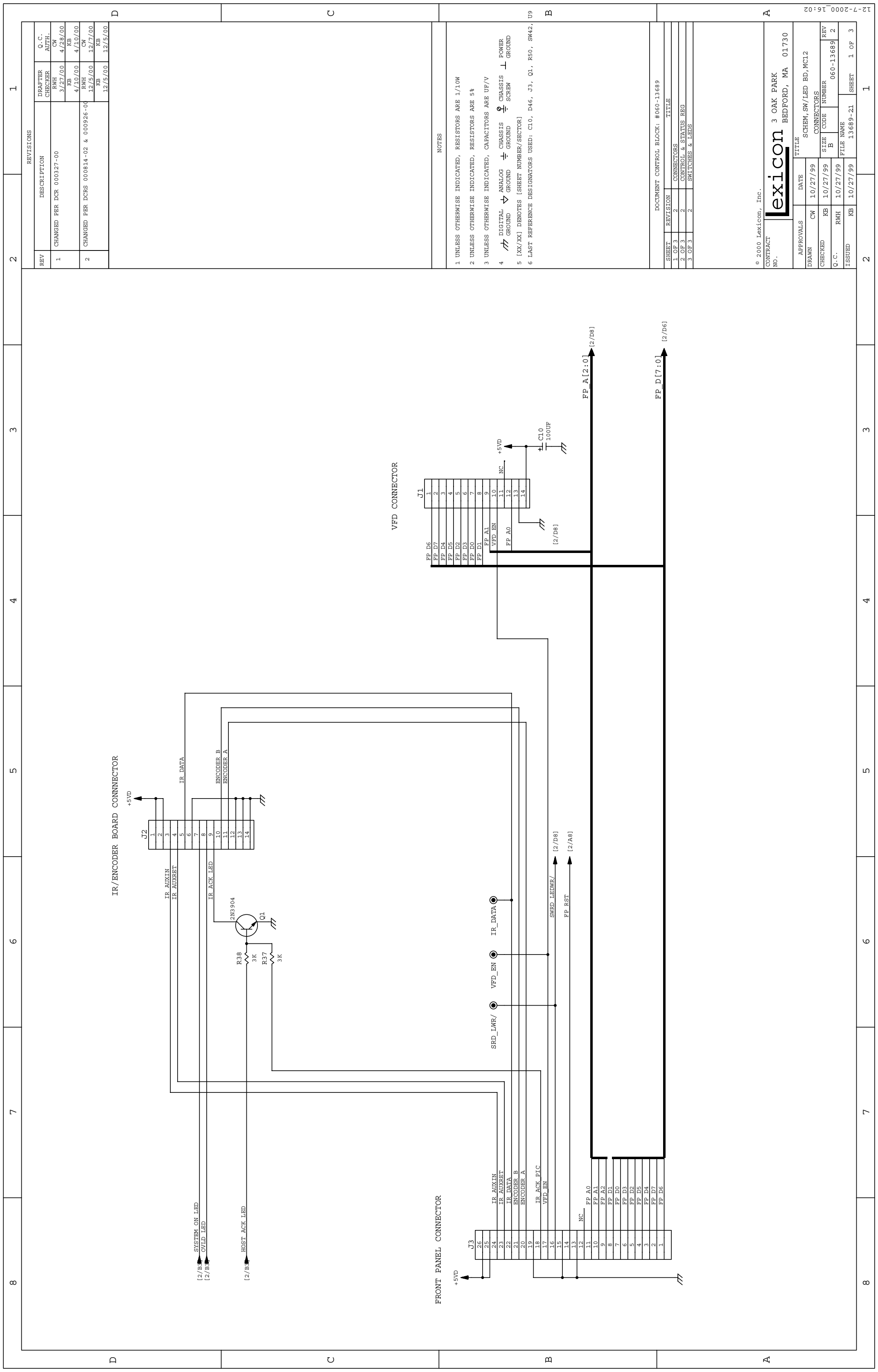
Your Notes:


CONTROL REGISTERS
74HC595
U5
U3
U4
MVID_SEL0
MVID_SEL1
MVID_SEL2
RVID_SEL0
RVID_SEL1
RVID_SEL2
NTSC_EN
PAL_EN
SECAM_EN
P_SEL0
P_SEL1
P_SEL2
P_SEL3
P_SEL4
QG
QH
NC
VREG_DATA
VREG_SCLK
VIDEO_RST/
VREG_RCLK
REVISIONS
REV
DESCRIPTION
DRAFTER CHECKER
Q.C. AUTH.
1 CHANGED PER DCR 000814-00
2 CHANGED PER DCR 001023-00
3 CHANGED PER DCRS 001205-00 AND 001222-01
lexicon 3 OAK PARK BEDFORD, MA 01730
CONTRACT NO.
APPROVALS
DATE
DRAWN RWH 12/1/99
CHECKED AP 1/13/00
Q.C. CW 1/14/00
ISSUED KB 1/17/00
TITLE
SCHEM,VIDEO BD,MC12
CONTROL REGISTERS
SIZE B
CODE
NUMBER 060-13679
REV 3
FILE NAME 13679-3.8
SHEET 8 OF 9
1-16-2001_12:36

Your Notes:

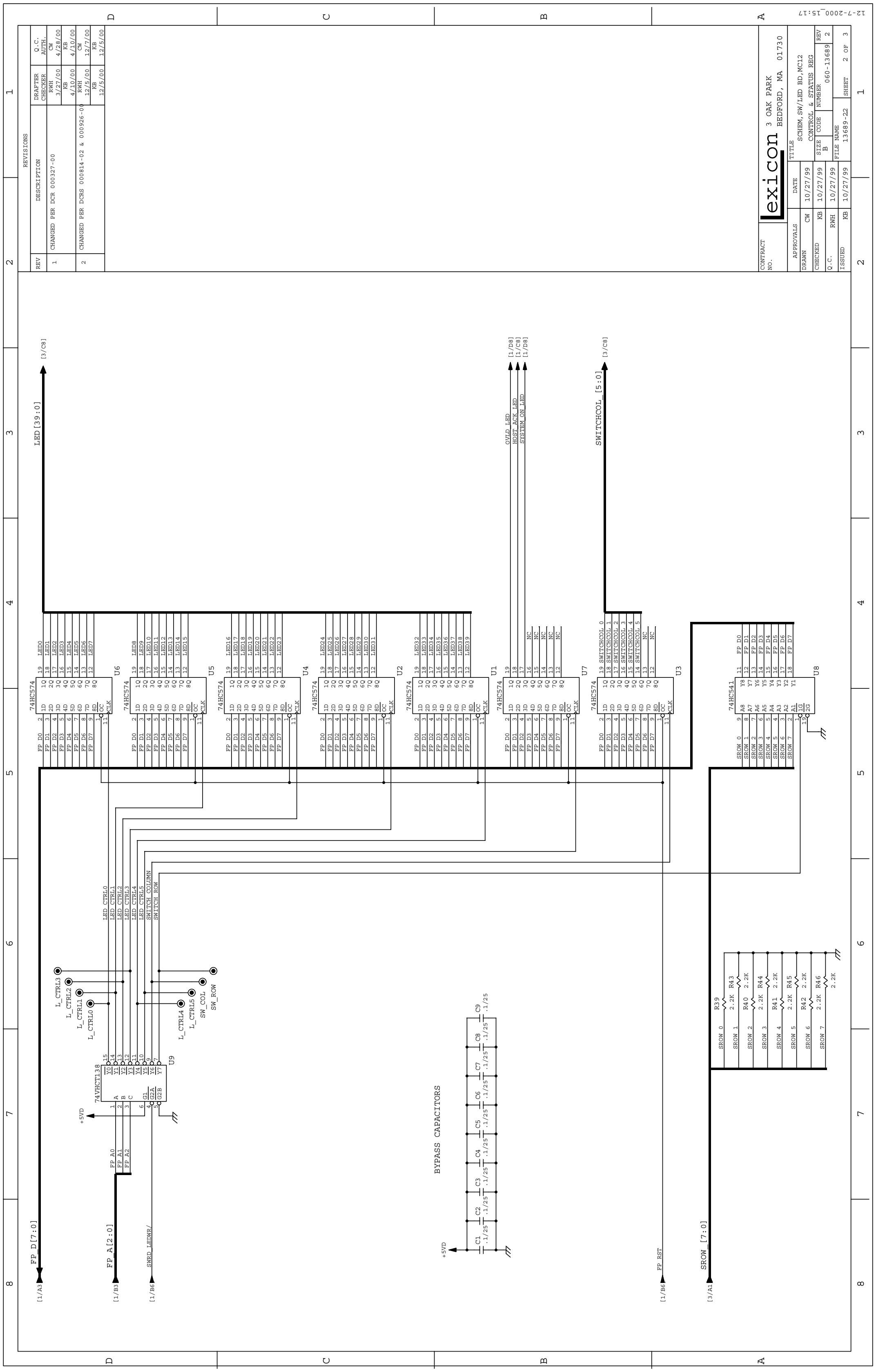

BYPASS CAPACITORS
MAIN BOARD CONNECTOR
POWER SUPPLY CONNECTOR (FROM ANALOG BOARD)
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,VIDEO BD,MC12
POWER AND CONTROL INTFC.
060-13679
SHEET 9 OF 9

Your Notes:

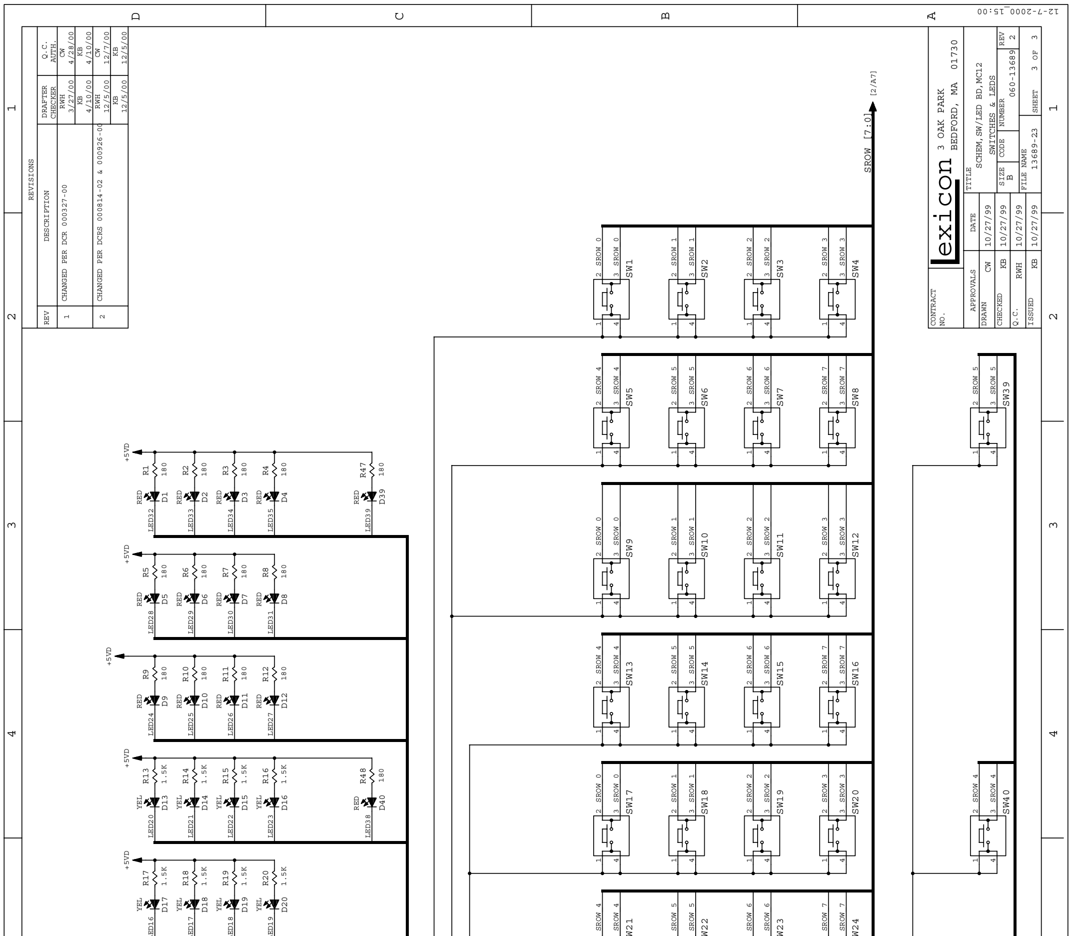


REVISIONS
REV
DESCRIPTION
DRAFTER CHECKER
Q.C. AUTH.
1 CHANGED PER DCR 000327-00
2 CHANGED PER DCRS 000814-02 & 000926-00
NOTES
1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W
2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%
3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V
4 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND CHASSIS SCREW POWER GROUND
5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]
6 LAST REFERENCE DESIGNATORS USED: C10, D46, J3, Q1, R50, SW42, U9
DOCUMENT CONTROL BLOCK: #060-13689
SHEET REVISION TITLE
1 OF 3 2 CONNECTORS
2 OF 3 2 CONTROL & STATUS REG
3 OF 3 2 SWITCHES & LEDS
© 2000 Lexicon, Inc.
lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE SCHEM,SW/LED BD,MC12 CONNECTORS
SIZE B
NUMBER 060-13689
REV 2
FILE NAME 13689-21
SHEET 1 OF 3
VFD CONNECTOR
J1
FP_A[2:0]
FP_D[7:0]
C10 100UF
+5VD
IR/ENCODER BOARD CONNECTOR
J2
IR_DATA
ENCODER_B
ENCODER_A
IR_AUXIN
IR_AUXRET
IR_ACK_LED
2N3904
Q1
R38 3K
R37 3K
IR_DATA
VFD_EN
SRD_LWR/
SWRD_LEDWR/
FP_RST
SYSTEM_ON_LED
OVLD_LED
HOST_ACK_LED
FRONT PANEL CONNECTOR
J3
IR_ACK_PIC
12-7-2000_16:02

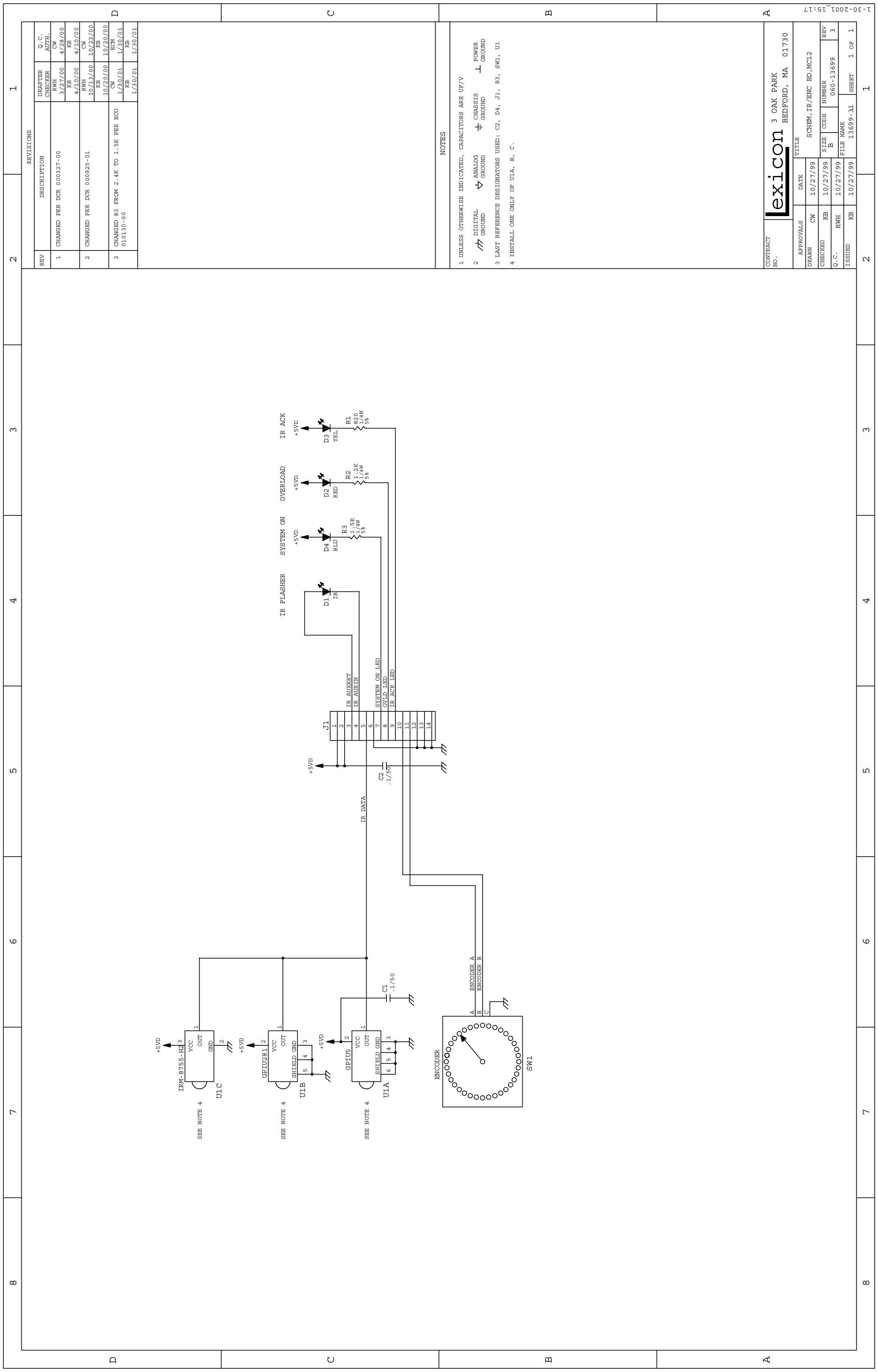
Your Notes:


REVISIONS
CHANGED PER DCR 000327-00
CHANGED PER DCRS 000814-02 & 000926-00
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,SW/LED BD,MC12
CONTROL & STATUS REG
060-13689
13689-22
2 OF 3
BYPASS CAPACITORS
LED[39:0]
SWITCHCOL [5:0]
FP D[7:0]
FP A[2:0]
SROW [7:0]

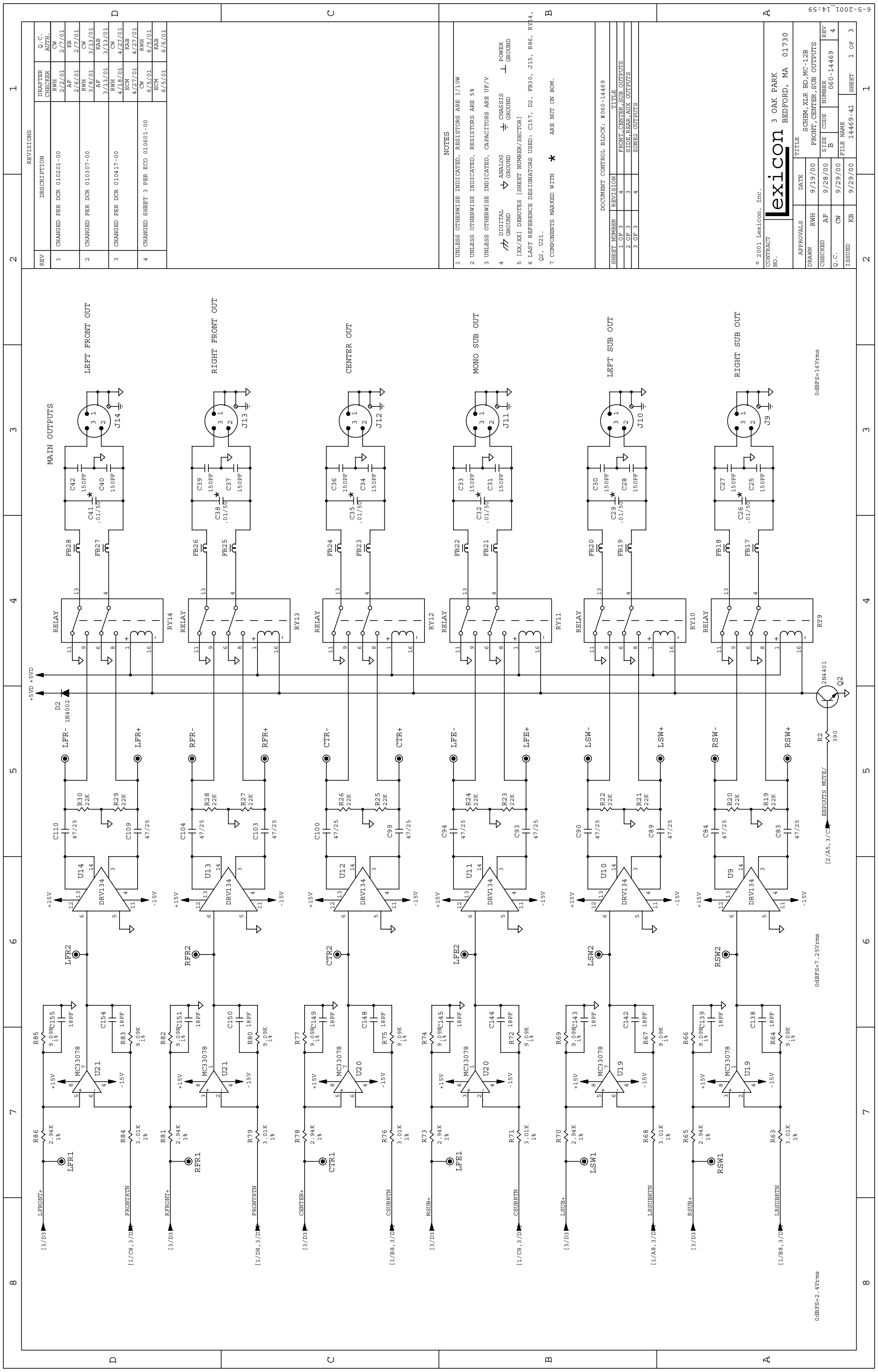
Your Notes:


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,SW/LED BD,MC12
SWITCHES & LEDS
060-13689
13689-23
SHEET 3 OF 3
SROW [7:0]
LED[39:0]
SWITCHCOL [5:0]

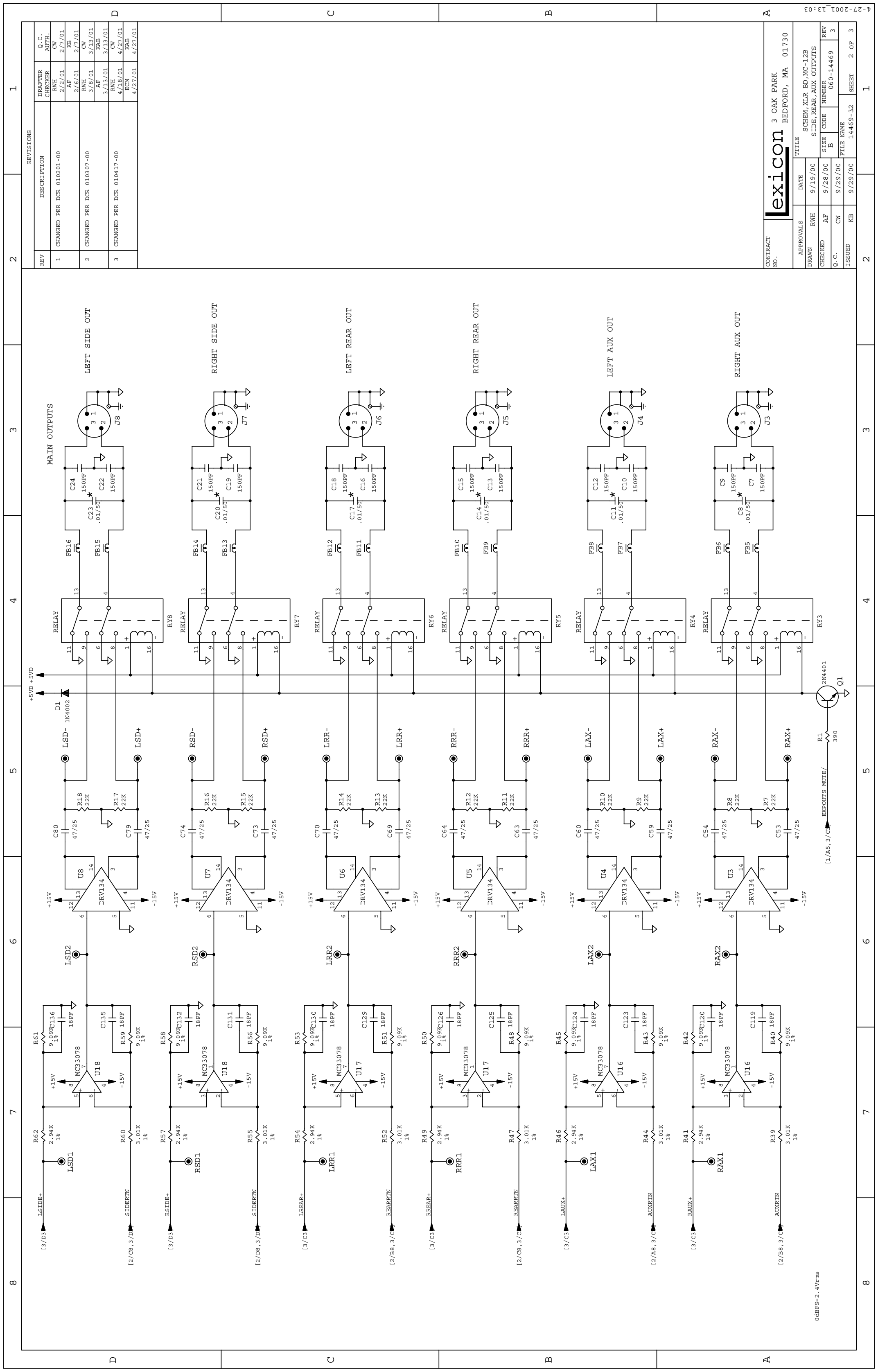
Your Notes:


REVISIONS
REV
DESCRIPTION
DRAFTER CHECKER
Q.C. AUTH.
1 CHANGED PER DCR 000327-00
2 CHANGED PER DCR 000925-01
3 CHANGED R3 FROM 2.4K TO 1.5K PER ECO 010130-00
NOTES
1 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V
2 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND
3 LAST REFERENCE DESIGNATORS USED: C2, D4, J1, R3, SW1, U1
4 INSTALL ONE ONLY OF U1A, B, C.
lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE SCHEM,IR/ENC BD,MC12
SIZE B
CODE
NUMBER 060-13699
REV 3
FILE NAME 13699-31
SHEET 1 OF 1
CONTRACT NO.
APPROVALS
DATE
DRAWN CW 10/27/99
CHECKED KB 10/27/99
Q.C. RWH 10/27/99
ISSUED KB 10/27/99
1-30-2001_15:17
IR ACK
OVERLOAD
SYSTEM ON
IR FLASHER
D1 IR
D2 RED
D3 YEL
D4 BLU
R1 820 1/4W 5%
R2 1.2K 1/4W 5%
R3 1.5K 1/4W 5%
+5VD
J1
IR AUXRET
IR AUXIN
SYSTEM ON LED
OVLD LED
IR ACK LED
C2 .1/50
IR DATA
C1 .1/50
ENCODER A
ENCODER B
ENCODER
SW1
IRM-8755-H2
GPIU281
GPIU5
VCC
OUT
GND
SHIELD GND
U1A
U1B
U1C
SEE NOTE 4

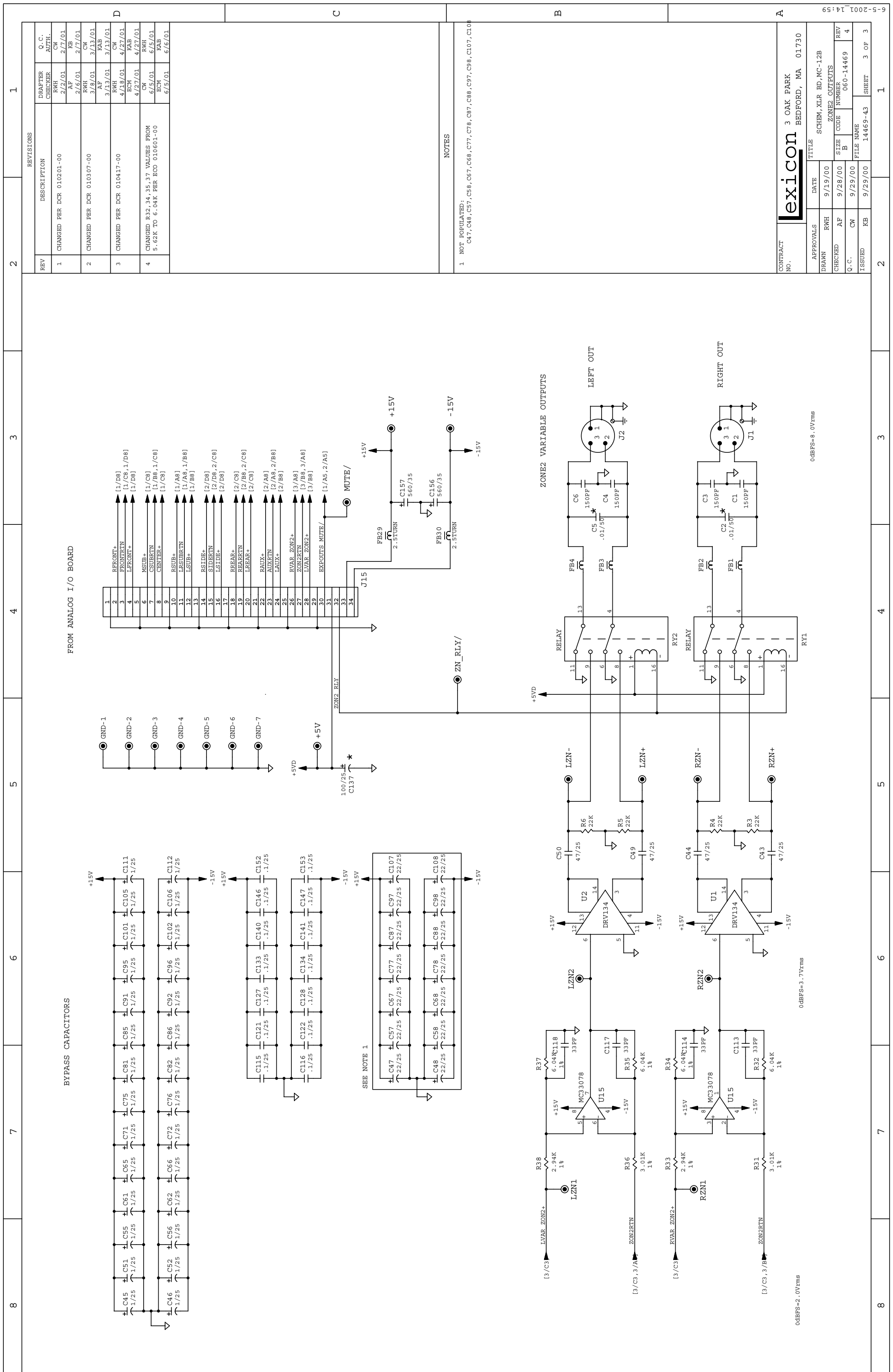
Your Notes:


MAIN OUTPUTS
LEFT FRONT OUT
RIGHT FRONT OUT
CENTER OUT
MONO SUB OUT
LEFT SUB OUT
RIGHT SUB OUT
REVISIONS
NOTES
lexicon 3 OAK PARK BEDFORD, MA 01730
SCHEM,XLR BD,MC-12B FRONT,CENTER,SUB OUTPUTS
060-14469
14469-41
© 2001 Lexicon, Inc.

Your Notes:

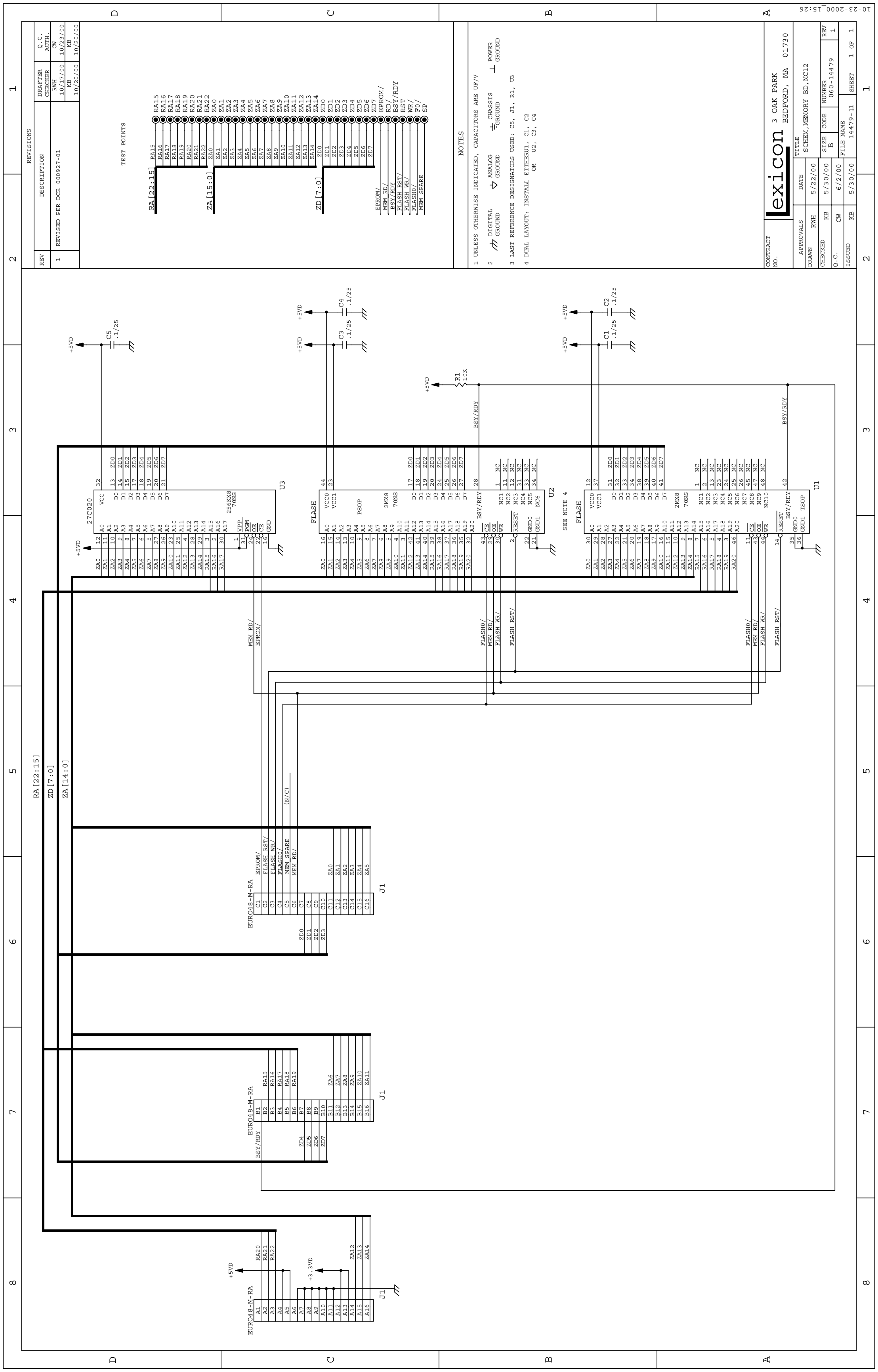

MAIN OUTPUTS
LEFT SIDE OUT
RIGHT SIDE OUT
LEFT REAR OUT
RIGHT REAR OUT
LEFT AUX OUT
RIGHT AUX OUT
REVISIONS
CHANGED PER DCR 010201-00
CHANGED PER DCR 010307-00
CHANGED PER DCR 010417-00
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,XLR BD,MC-12B
SIDE,REAR,AUX OUTPUTS
060-14469
14469-32
SHEET 2 OF 3

Your Notes:

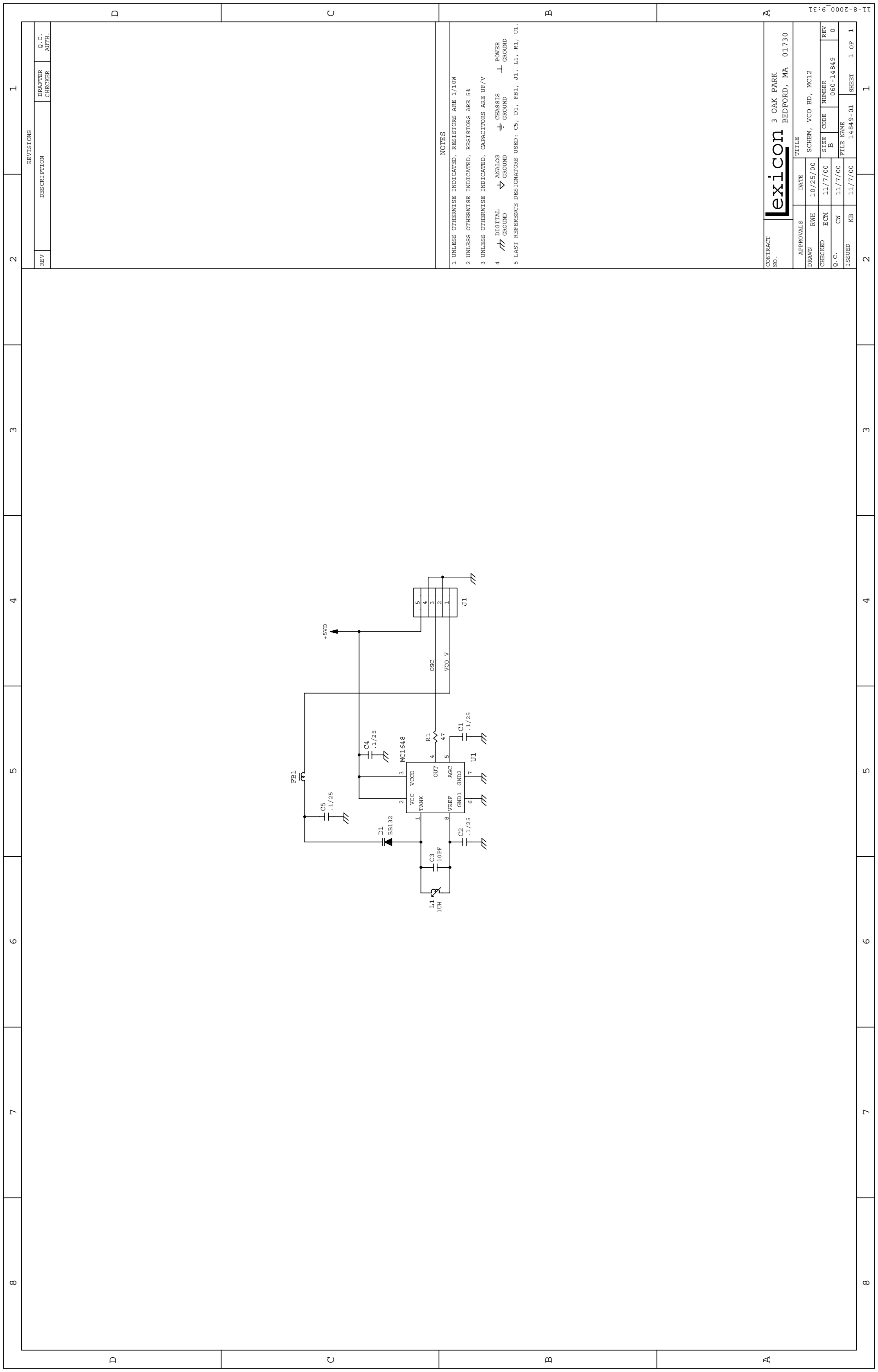


lexicon 3 OAK PARK
BEDFORD, MA 01730
SCHEM,XLR BD,MC-12B
ZONE2 OUTPUTS
060-14469
14469-43
SHEET 3 OF 3
REVISIONS
NOTES
1 NOT POPULATED:
FROM ANALOG I/O BOARD
BYPASS CAPACITORS
ZONE2 VARIABLE OUTPUTS
LEFT OUT
RIGHT OUT

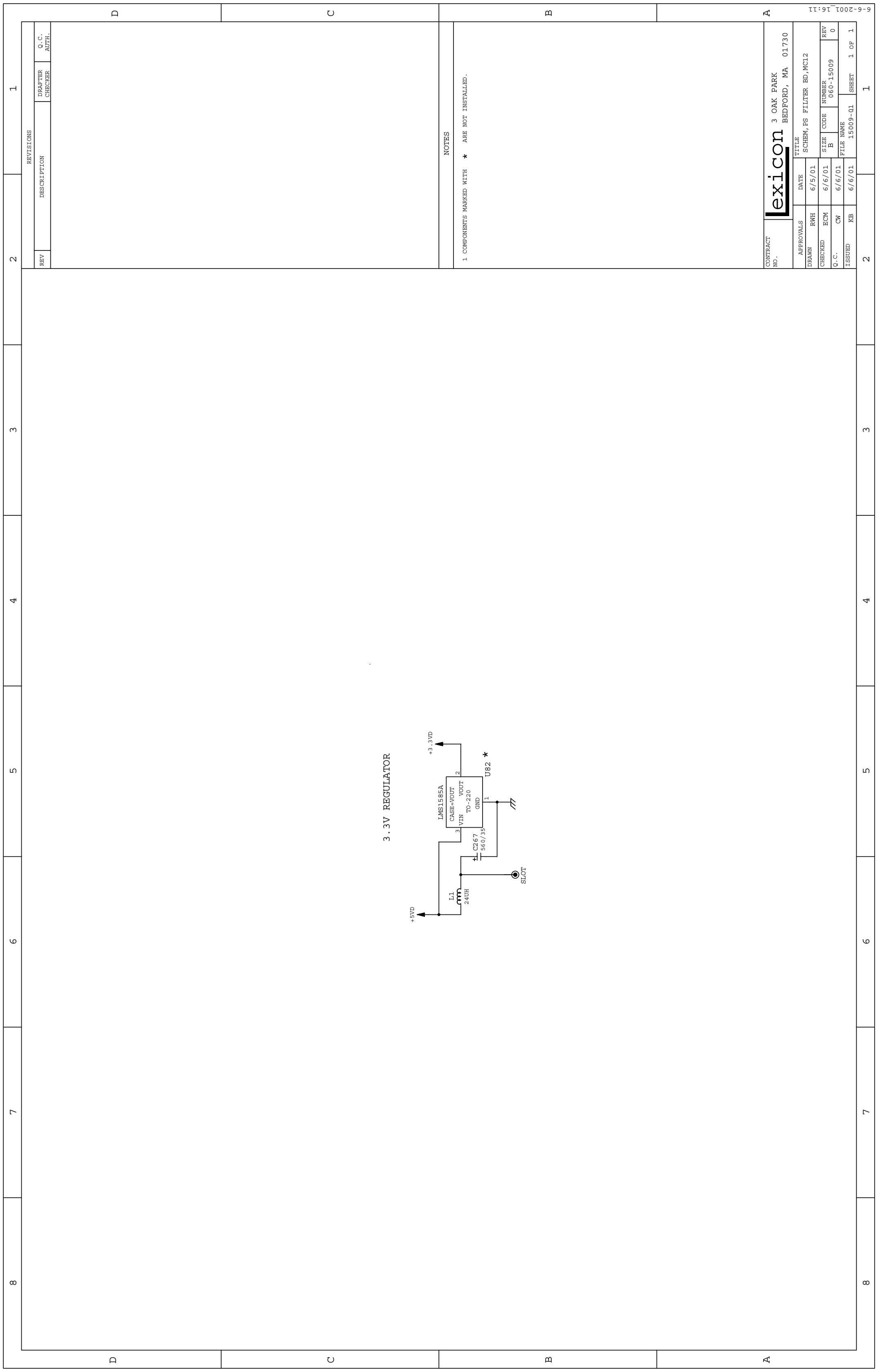
Your Notes:


NOTES
1 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V
2 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND
3 LAST REFERENCE DESIGNATORS USED: C5, J1, R1, U3
4 DUAL LAYOUT: INSTALL EITHER U1, C1, C2 OR U2, C3, C4
TEST POINTS
REVISIONS
1 REVISED PER DCR 000927-01
lexicon 3 OAK PARK BEDFORD, MA 01730
TITLE SCHEM,MEMORY BD,MC12
SIZE B
NUMBER 060-14479
REV 1
FILE NAME 14479-11
SHEET 1 OF 1
27C020
FLASH
EURO48-M-RA
J1
U1
U2
U3
10-23-2000_15:26

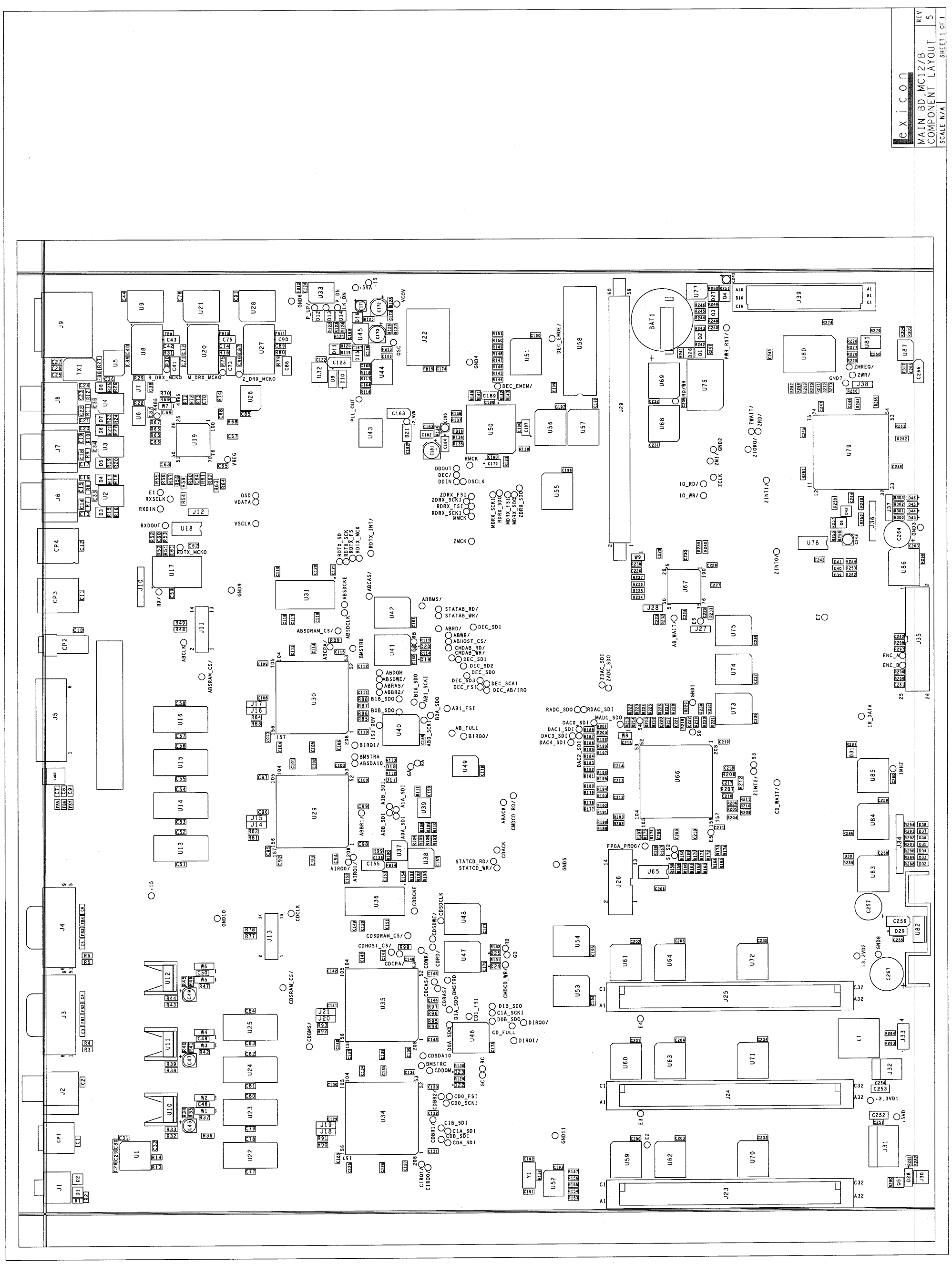
Your Notes:


REVISIONS
REV
DESCRIPTION
DRAFTER CHECKER
Q.C. AUTH.
NOTES
1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W
2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%
3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V
4 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND
5 LAST REFERENCE DESIGNATORS USED: C5, D1, FB1, J1, L1, R1, U1.
lexicon 3 OAK PARK BEDFORD, MA 01730
CONTRACT NO.
APPROVALS DATE
DRAWN RWH 10/25/00
CHECKED ECM 11/7/00
Q.C. CW 11/7/00
ISSUED KB 11/7/00
TITLE SCHEM, VCO BD, MC12
SIZE B
CODE
NUMBER 060-14849
REV 0
FILE NAME 14849-01
SHEET 1 OF 1
11-8-2000_9:31
+5VD
OSC
VCO_V
J1
R1 47
C1 .1/25
C4 .1/25
MC1648
U1
VCC VCCO OUT AGC TANK VREF GND1 GND2
FB1
C5 .1/25
D1 BB132
C2 .1/25
C3 10PF
L1 1UH

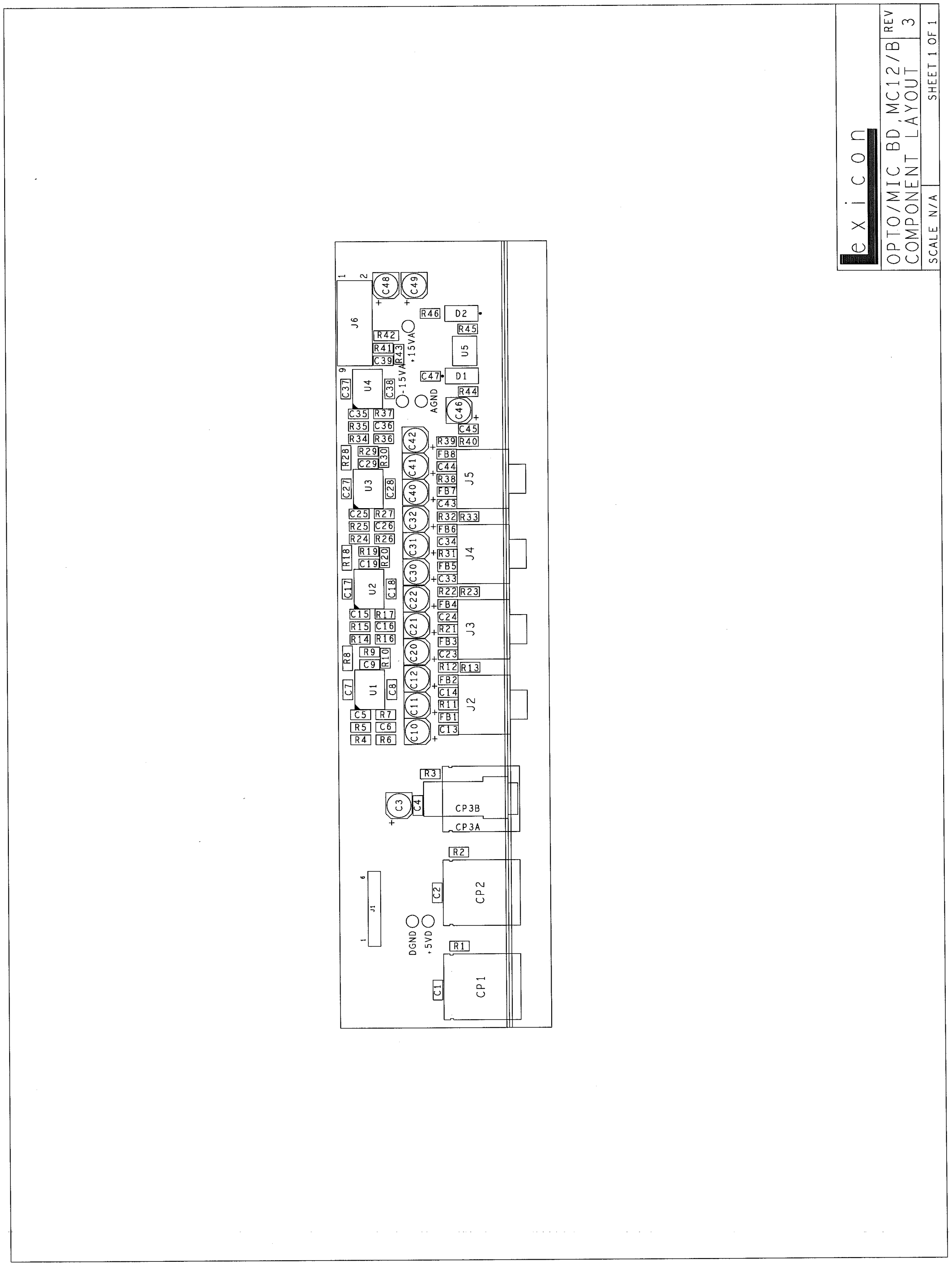
Your Notes:


3.3V REGULATOR
LMS1585A
CASE=VOUT
VIN
VOUT
TO-220
GND
U82 *
+3.3VD
+5VD
L1
24UH
C267
560/35
SLOT
REVISIONS
REV
DESCRIPTION
DRAFTER
CHECKER
Q.C.
AUTH.
NOTES
1 COMPONENTS MARKED WITH * ARE NOT INSTALLED.
lexicon
3 OAK PARK
BEDFORD, MA 01730
CONTRACT NO.
APPROVALS
DATE
DRAWN RWH 6/5/01
CHECKED ECM 6/6/01
Q.C. CW 6/6/01
ISSUED KB 6/6/01
TITLE
SCHEM,PS FILTER BD,MC12
SIZE B
CODE
NUMBER 060-15009
REV 0
FILE NAME 15009-01
SHEET 1 OF 1
6-6-2001_16:11

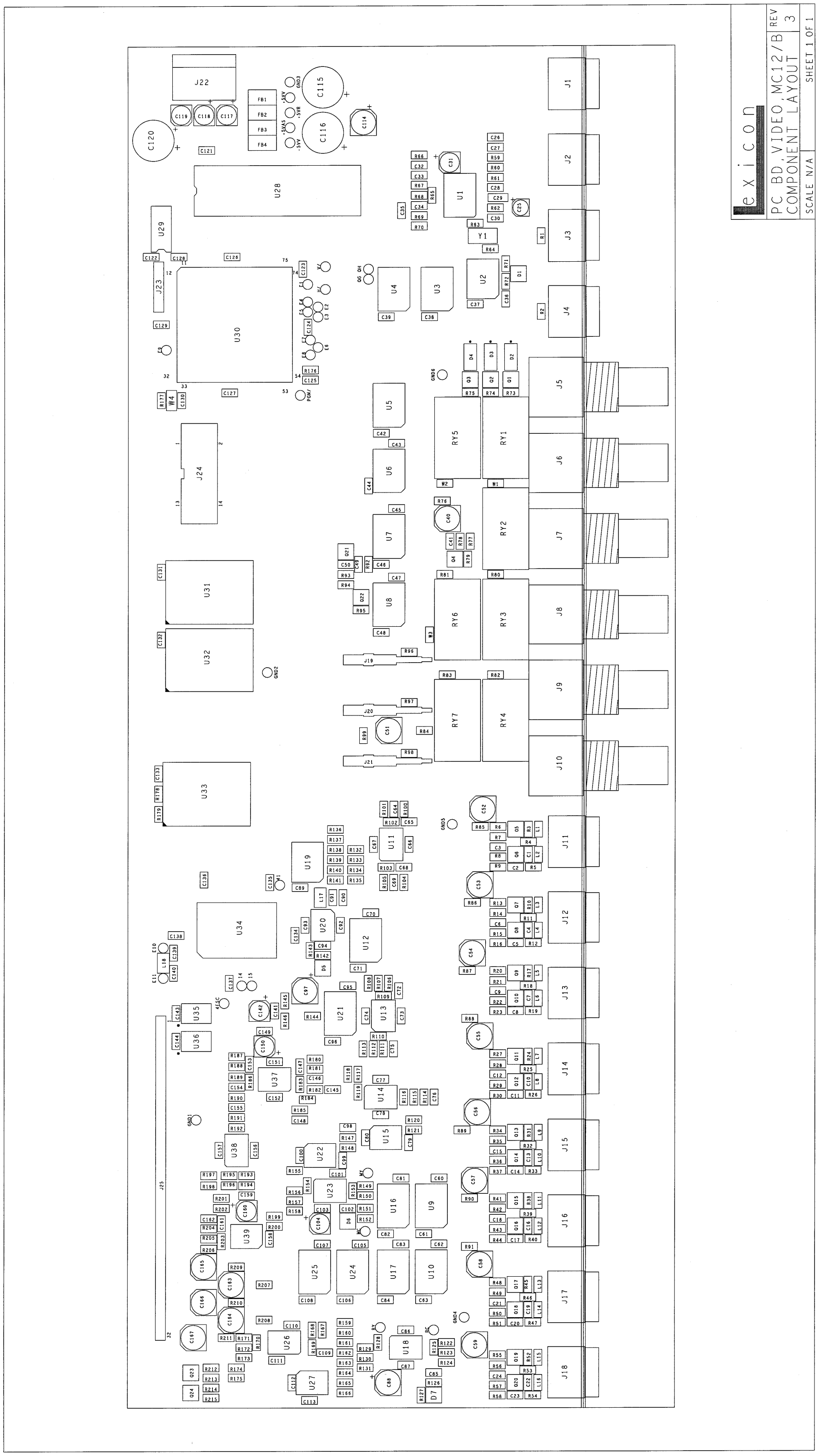
Your Notes:


lexicon
MAIN BD MC12/B
COMPONENT LAYOUT
REV
5
SCALE N/A
SHEET 1 OF 1

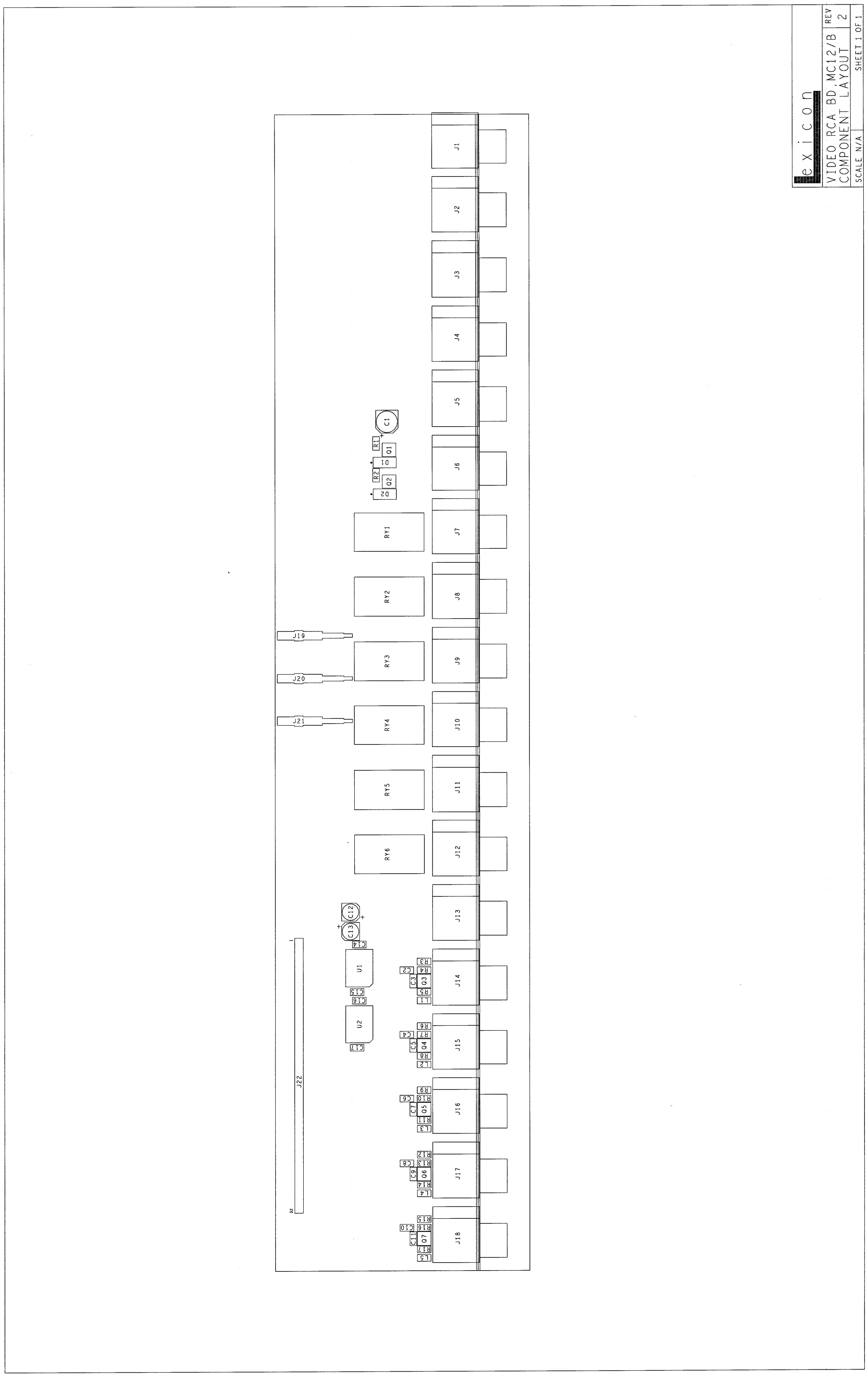
Your Notes:


lexicon
OPTO/MIC BD, MC12/B
COMPONENT LAYOUT
REV
3
SCALE N/A
SHEET 1 OF 1

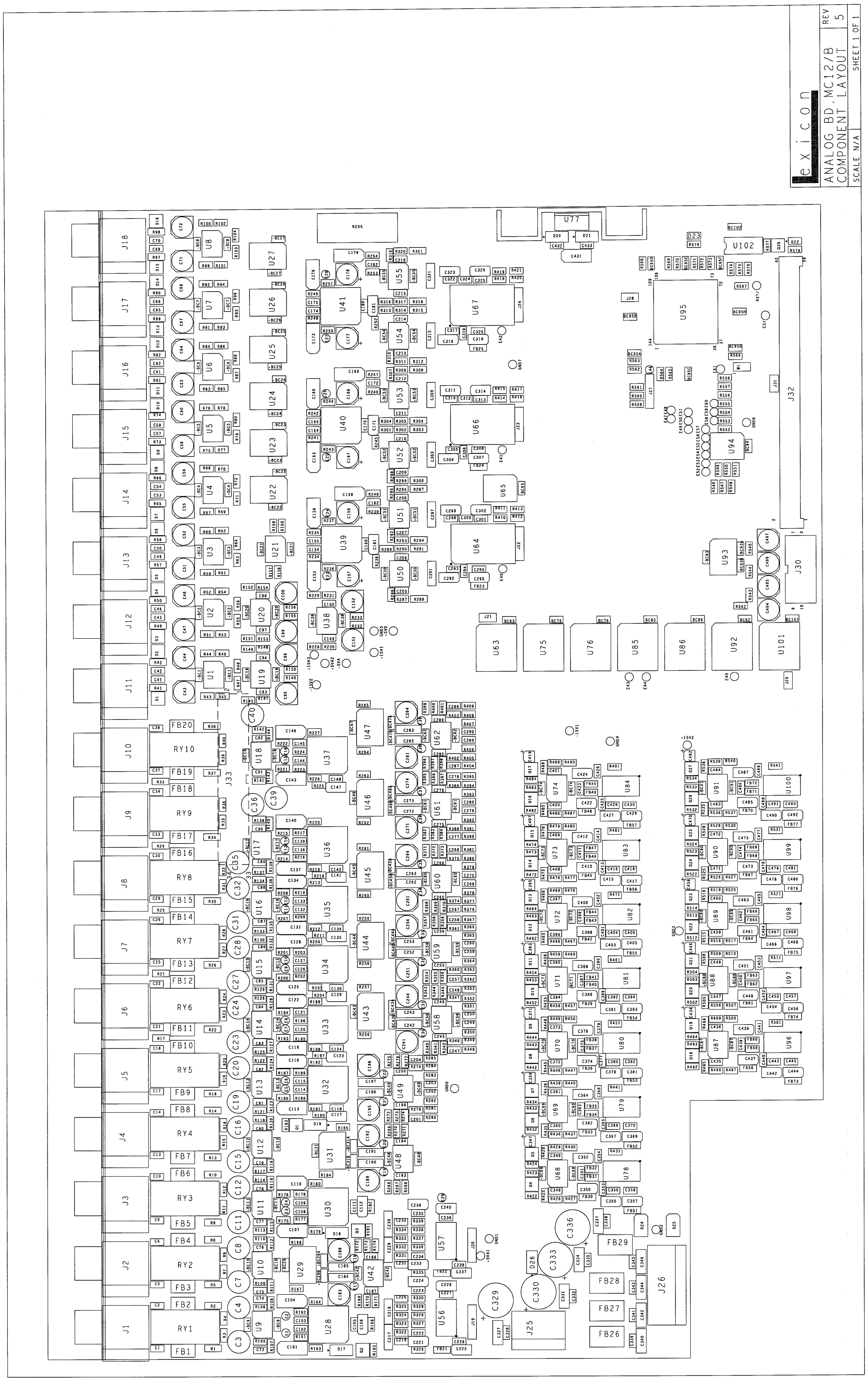
Your Notes:


lexicon
PC BD, VIDEO, MC12/B
COMPONENT LAYOUT
REV
3
SCALE N/A
SHEET 1 OF 1

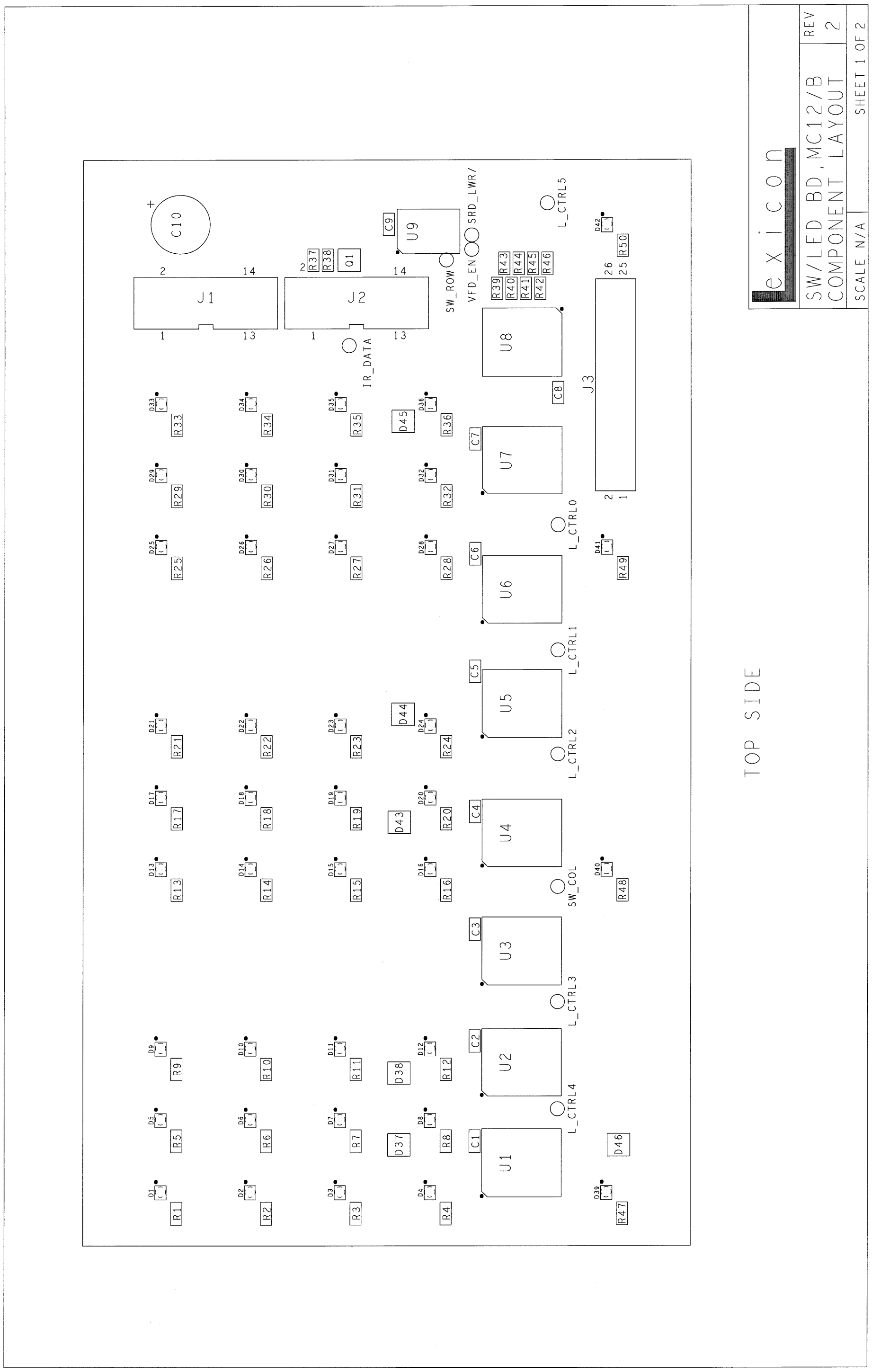
Your Notes:


lexicon
VIDEO RCA BD. MC12/B
COMPONENT LAYOUT
REV
2
SCALE N/A
SHEET 1 OF 1

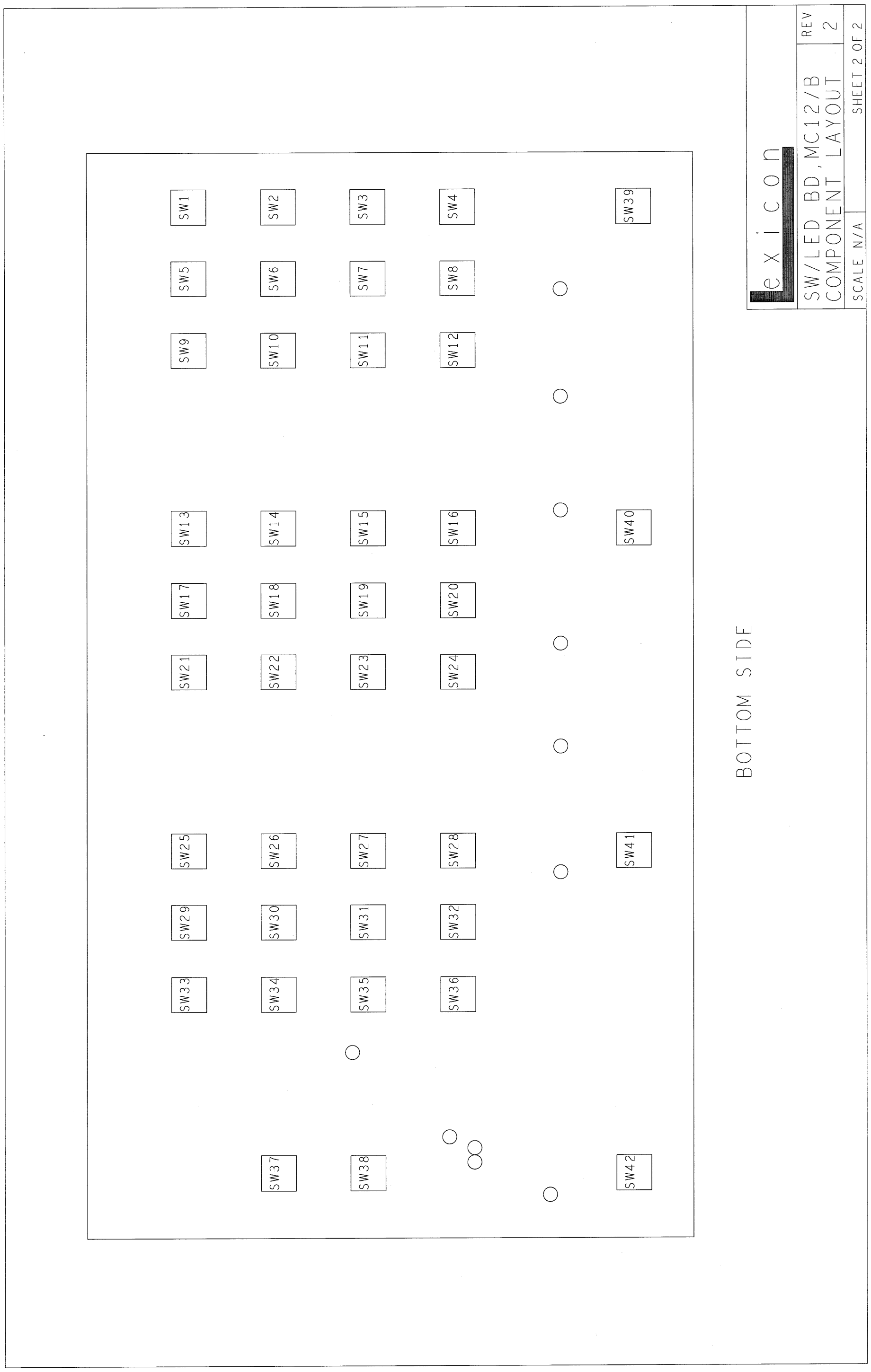
Your Notes:


lexicon
ANALOG BD, MC12/B
COMPONENT LAYOUT
REV
5
SCALE N/A
SHEET 1 OF 1

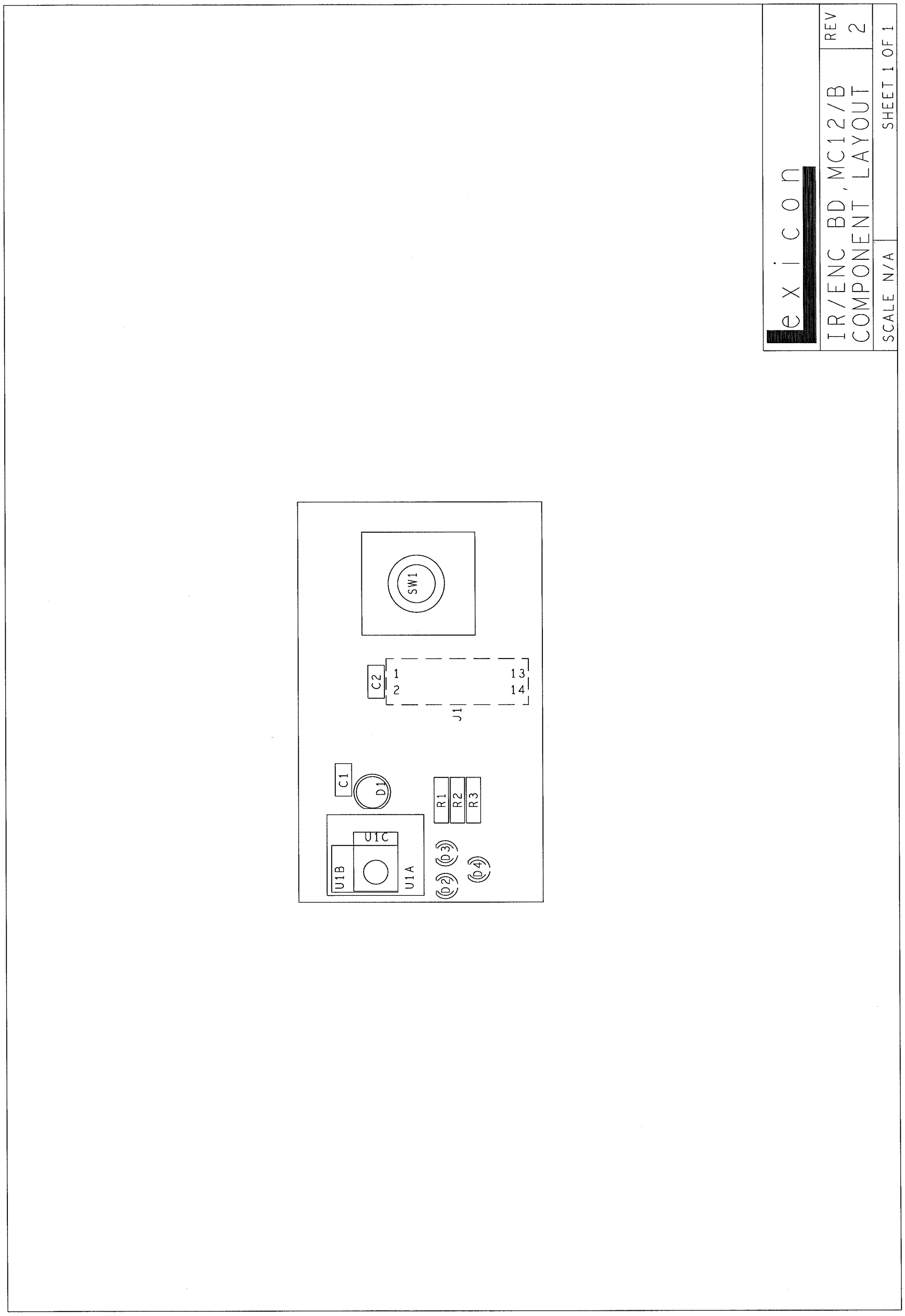
Your Notes:


lexicon
SW/LED BD, MC12/B
COMPONENT LAYOUT
REV 2
SCALE N/A
SHEET 1 OF 2
TOP SIDE

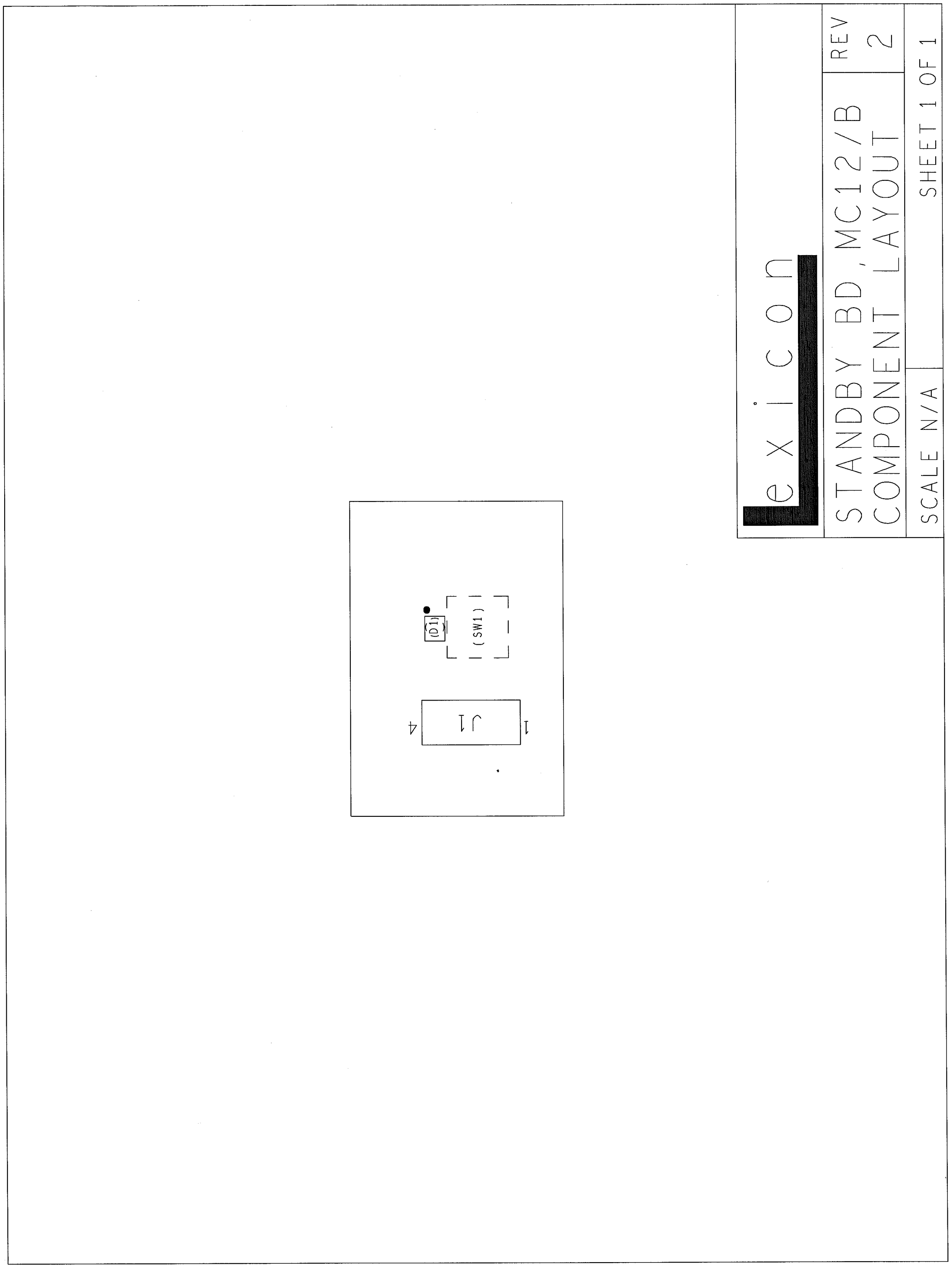
Your Notes:


lexicon
SW/LED BD,MC12/B
COMPONENT LAYOUT
REV
2
SCALE N/A
SHEET 2 OF 2
BOTTOM SIDE
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
SW13
SW14
SW15
SW16
SW17
SW18
SW19
SW20
SW21
SW22
SW23
SW24
SW25
SW26
SW27
SW28
SW29
SW30
SW31
SW32
SW33
SW34
SW35
SW36
SW37
SW38
SW39
SW40
SW41
SW42

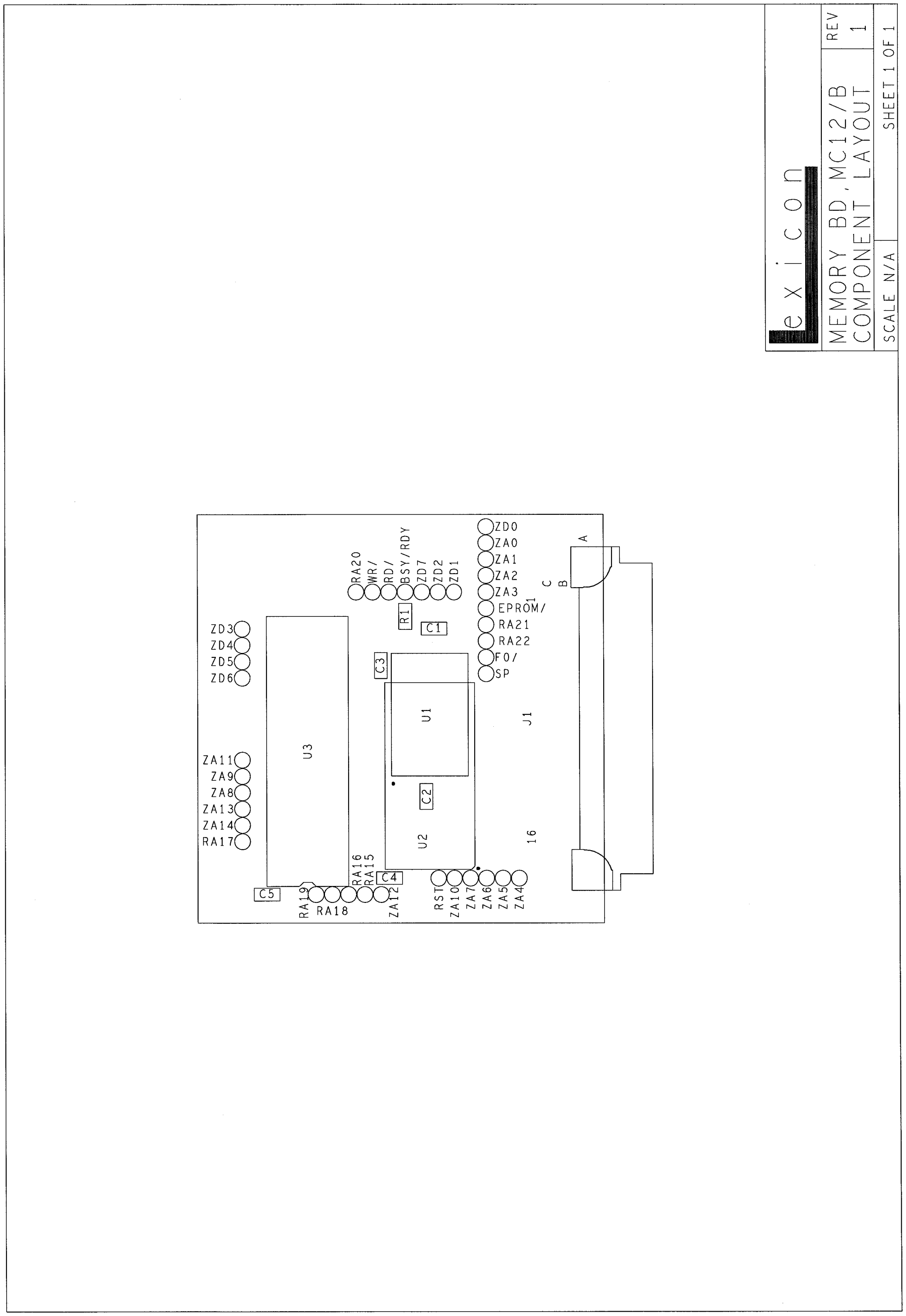
Your Notes:


lexicon
IR/ENC BD, MC12/B
COMPONENT LAYOUT
REV
2
SCALE N/A
SHEET 1 OF 1
SW1
C2
1
2
13
14
J1
C1
D1
R1
R2
R3
U1C
U1B
U1A
D2
D3
D4

Your Notes:

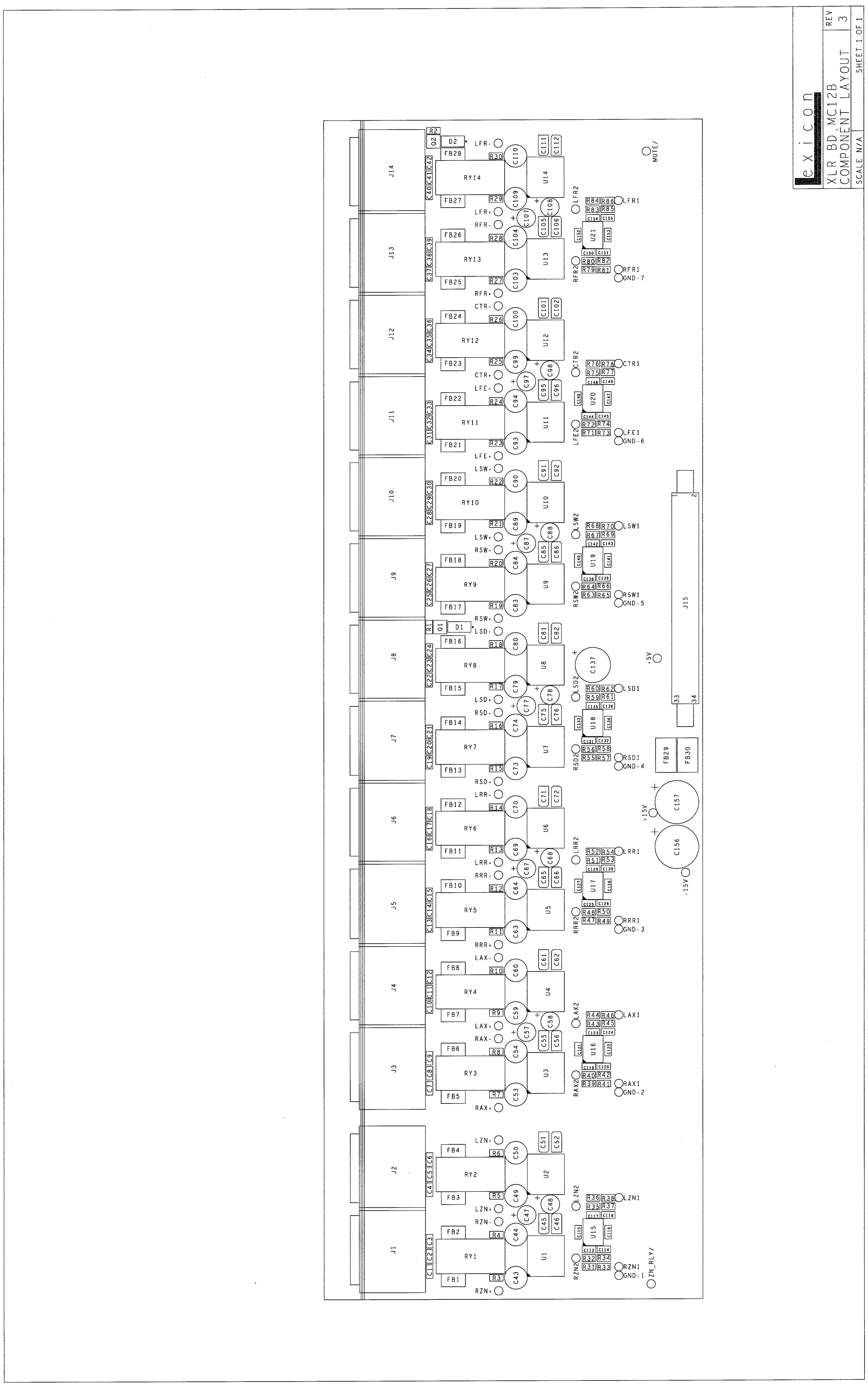

lexicon
STANDBY BD, MC12/B
COMPONENT LAYOUT
REV
2
SCALE N/A
SHEET 1 OF 1
(D1)
(SW1)
J1
4
1

Your Notes:

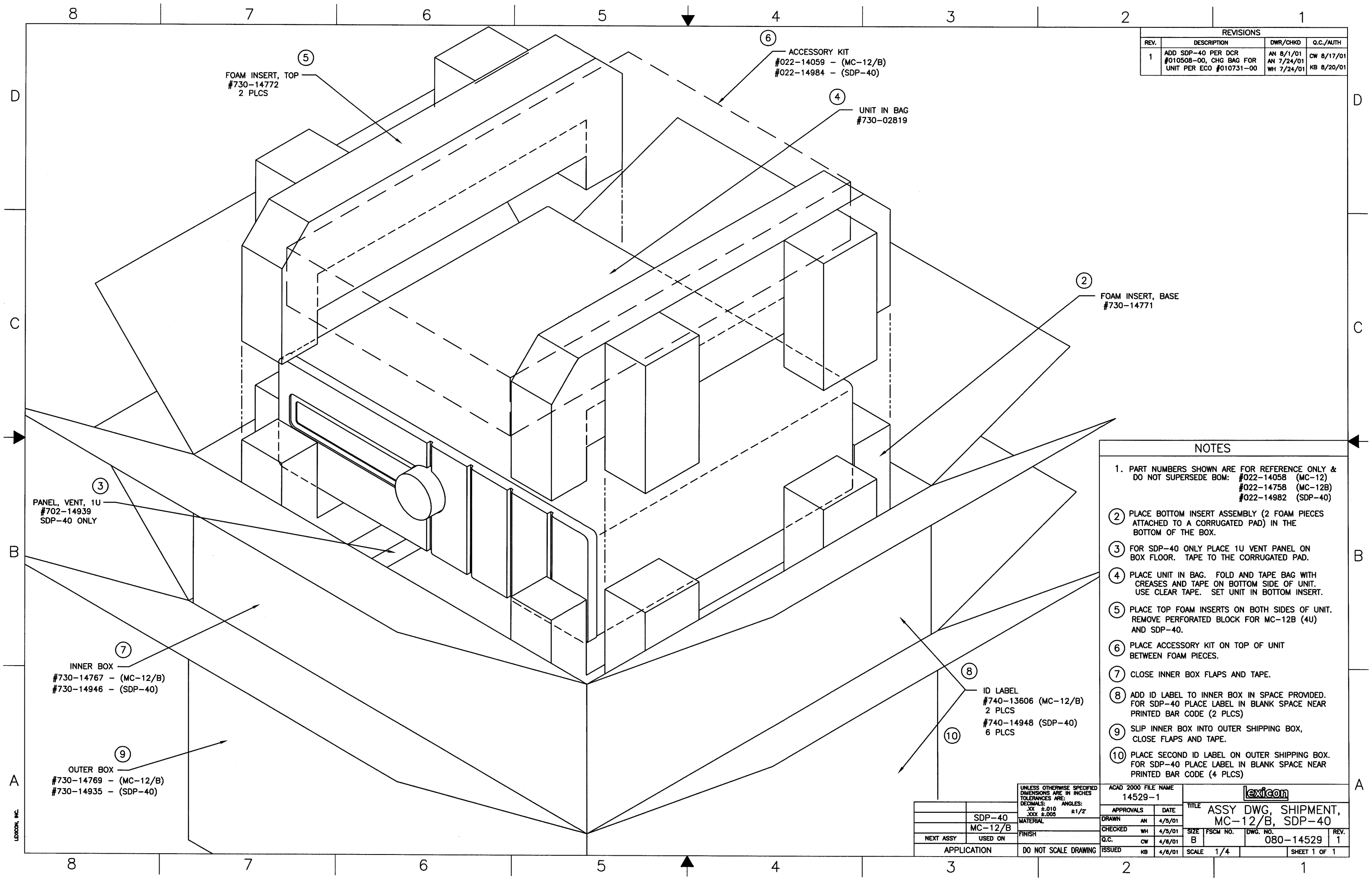


lexicon
MEMORY BD,MC12/B
COMPONENT LAYOUT
REV
1
SCALE N/A
SHEET 1 OF 1
U1
U2
U3
J1
C1
C2
C3
C4
C5
R1
ZD0
ZA0
ZA1
ZA2
ZA3
EPROM/
RA21
RA22
F0/
SP
RA20
WR/
RD/
BSY/RDY
ZD7
ZD2
ZD1
ZD3
ZD4
ZD5
ZD6
ZA11
ZA9
ZA8
ZA13
ZA14
RA17
RA19
RA18
RA16
RA15
ZA12
RST
ZA10
ZA7
ZA6
ZA5
ZA4
A
B
C
1
16

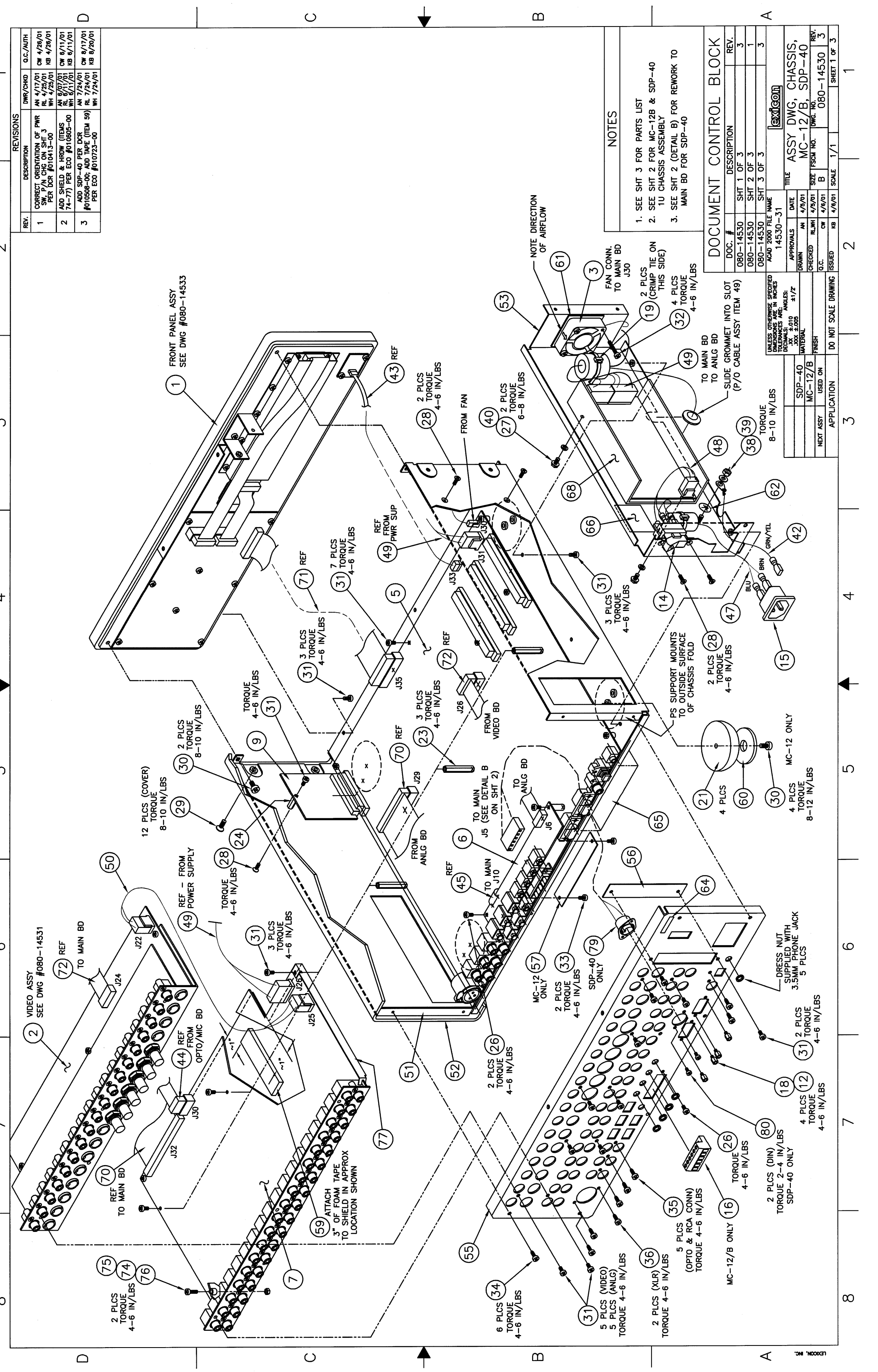
Your Notes:


lexicon
XLR BD, MC12B
COMPONENT LAYOUT
REV
3
SCALE N/A
SHEET 1 OF 1

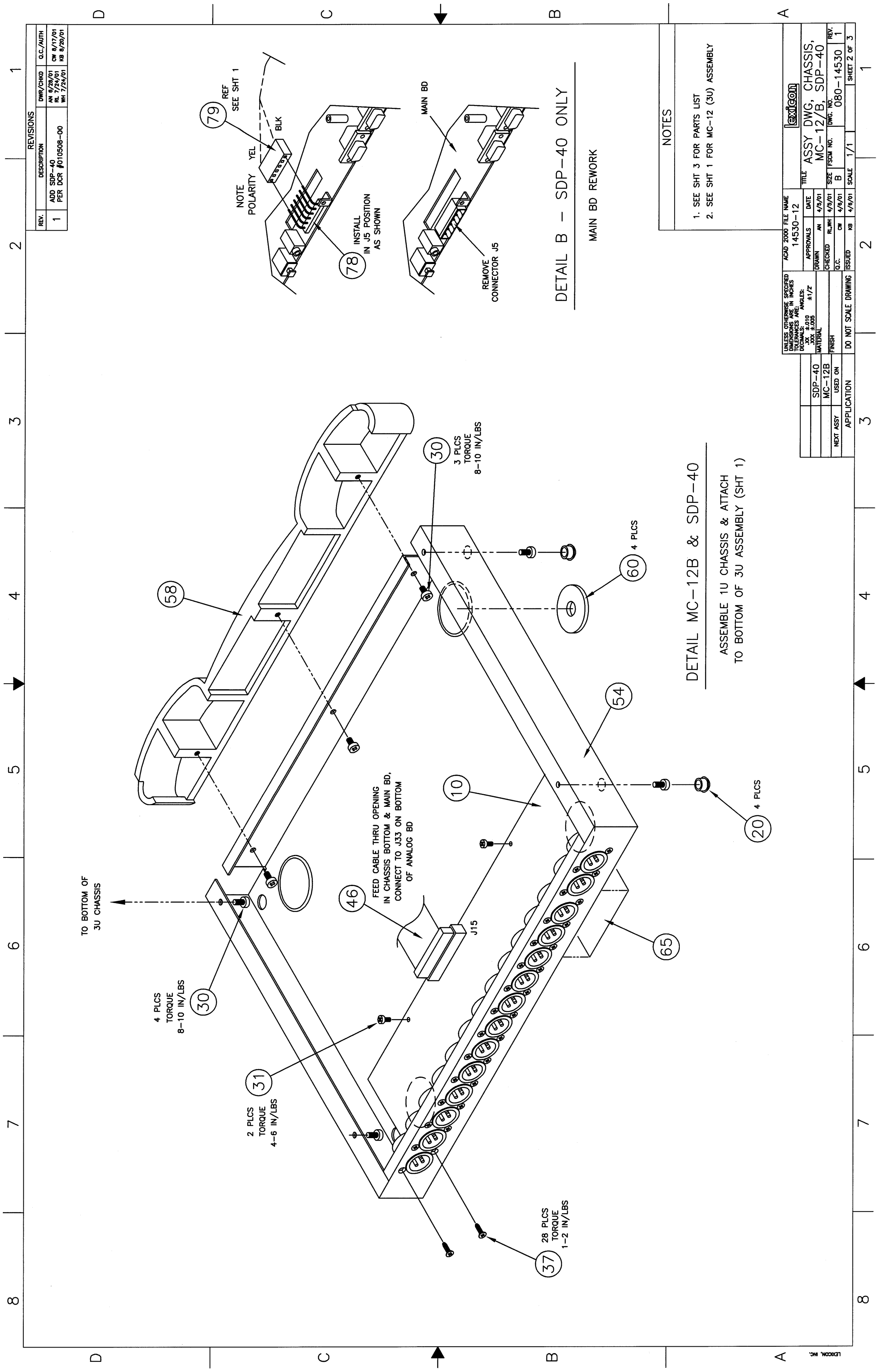
Your Notes:


REVISIONS
REV. | DESCRIPTION | DWR/CHKD | Q.C./AUTH
1 | ADD SDP-40 PER DCR #010508-00, CHG BAG FOR UNIT PER ECO #010731-00 | AN 8/1/01 AN 7/24/01 WH 7/24/01 | CW 8/17/01 KB 8/20/01
5 FOAM INSERT, TOP #730-14772 2 PLCS
6 ACCESSORY KIT #022-14059 - (MC-12/B) #022-14984 - (SDP-40)
4 UNIT IN BAG #730-02819
2 FOAM INSERT, BASE #730-14771
3 PANEL, VENT, 1U #702-14939 SDP-40 ONLY
7 INNER BOX #730-14767 - (MC-12/B) #730-14946 - (SDP-40)
9 OUTER BOX #730-14769 - (MC-12/B) #730-14935 - (SDP-40)
8 10 ID LABEL #740-13606 (MC-12/B) 2 PLCS #740-14948 (SDP-40) 6 PLCS
NOTES
1. PART NUMBERS SHOWN ARE FOR REFERENCE ONLY & DO NOT SUPERSEDE BOM: #022-14058 (MC-12) #022-14758 (MC-12B) #022-14982 (SDP-40)
2 PLACE BOTTOM INSERT ASSEMBLY (2 FOAM PIECES ATTACHED TO A CORRUGATED PAD) IN THE BOTTOM OF THE BOX.
3 FOR SDP-40 ONLY PLACE 1U VENT PANEL ON BOX FLOOR. TAPE TO THE CORRUGATED PAD.
4 PLACE UNIT IN BAG. FOLD AND TAPE BAG WITH CREASES AND TAPE ON BOTTOM SIDE OF UNIT. USE CLEAR TAPE. SET UNIT IN BOTTOM INSERT.
5 PLACE TOP FOAM INSERTS ON BOTH SIDES OF UNIT. REMOVE PERFORATED BLOCK FOR MC-12B (4U) AND SDP-40.
6 PLACE ACCESSORY KIT ON TOP OF UNIT BETWEEN FOAM PIECES.
7 CLOSE INNER BOX FLAPS AND TAPE.
8 ADD ID LABEL TO INNER BOX IN SPACE PROVIDED. FOR SDP-40 PLACE LABEL IN BLANK SPACE NEAR PRINTED BAR CODE (2 PLCS)
9 SLIP INNER BOX INTO OUTER SHIPPING BOX, CLOSE FLAPS AND TAPE.
10 PLACE SECOND ID LABEL ON OUTER SHIPPING BOX. FOR SDP-40 PLACE LABEL IN BLANK SPACE NEAR PRINTED BAR CODE (4 PLCS)
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING
SDP-40
MC-12/B
NEXT ASSY | USED ON
APPLICATION
ACAD 2000 FILE NAME 14529-1
APPROVALS | DATE
DRAWN AN 4/5/01
CHECKED WH 4/5/01
Q.C. CW 4/6/01
ISSUED KB 4/6/01
lexicon
TITLE ASSY DWG, SHIPMENT, MC-12/B, SDP-40
SIZE B | FSCM NO. | DWG. NO. 080-14529 | REV. 1
SCALE 1/4 | SHEET 1 OF 1
LEXICON, INC.

Your Notes:


NOTES
1. SEE SHT 3 FOR PARTS LIST
2. SEE SHT 2 FOR MC-12B & SDP-40 1U CHASSIS ASSEMBLY
3. SEE SHT 2 (DETAIL B) FOR REWORK TO MAIN BD FOR SDP-40
DOCUMENT CONTROL BLOCK
ASSY DWG, CHASSIS, MC-12/B, SDP-40
080-14530
DO NOT SCALE DRAWING
FRONT PANEL ASSY SEE DWG #080-14533
VIDEO ASSY SEE DWG #080-14531
NOTE DIRECTION OF AIRFLOW

Your Notes:


REVISIONS
REV. | DESCRIPTION | DWR/CHKD | Q.C./AUTH
1 | ADD SDP-40 PER DCR #010508-00 | AN 7/25/01 RL 7/24/01 WH 7/24/01 | CW 8/17/01 KB 8/20/01
NOTES
1. SEE SHT 3 FOR PARTS LIST
2. SEE SHT 1 FOR MC-12 (3U) ASSEMBLY
DETAIL B - SDP-40 ONLY
MAIN BD REWORK
NOTE POLARITY
YEL
BLK
REF SEE SHT 1
INSTALL IN J5 POSITION AS SHOWN
MAIN BD
REMOVE CONNECTOR J5
DETAIL MC-12B & SDP-40
ASSEMBLE 1U CHASSIS & ATTACH TO BOTTOM OF 3U ASSEMBLY (SHT 1)
3 PLCS TORQUE 8-10 IN/LBS
4 PLCS
TO BOTTOM OF 3U CHASSIS
4 PLCS TORQUE 8-10 IN/LBS
FEED CABLE THRU OPENING IN CHASSIS BOTTOM & MAIN BD, CONNECT TO J33 ON BOTTOM OF ANALOG BD
J15
2 PLCS TORQUE 4-6 IN/LBS
28 PLCS TORQUE 1-2 IN/LBS
4 PLCS
ASSY DWG, CHASSIS, MC-12/B, SDP-40
ACAD 2000 FILE NAME 14530-12
SDP-40
MC-12B
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING
SIZE B
DWG. NO. 080-14530
REV. 1
SCALE 1/1
SHEET 2 OF 3

Your Notes:

ITEM#	PART#	DESCRIPTION	QTY	WHERE USED
1.	022-14990 022-14986	PL, MECH ASSY, FP, MC12/B PL, MECH ASSY, FP, SDP40	1	
2.	022-14782	PL, FINAL ASSY, VIDEO	1	
3.	022-14850	PL, FAN ASSY	1	
4.				
5.	023-14781 023-14988	PL, MAIN BD ASSY, MC12/B PL, MAIN BD ASSY, SDP40	1	
6.	023-14063	PL, OPTO/MIC BD ASSY	1	
7.	023-14066	PL, ANLG I/O BD ASSY	1	
8.				
9.	023-14783 023-14987	PL, MEMORY BD ASSY, MC12/B PL, MEMORY BD ASSY, SDP40	1	
10.	023-14078	PL, XLR BD ASSY	1	(12B & SDP40 ONLY)
11.				
12.	120-09621	LOCTITE #242	–	D CONN JSCKT
13.				
14.	454-13850	SWITCH, ROCKER	1	
15.	490-11462	CONN, AC, 3C, SNAP, IEC	1	
16.	490-13872	CONN, PLUG, .200, 6FC, RA	1	(MC12 &12B ONLY)
17.				
18.	527-12974	CONN, DSUB, JSCKT, 4-40	4	D CONN TO REAR PNL
19.	530-02488	TIE, CABLE, NYL	2	FERRITE SLV TO PS SPRT
20.	540-02472	PLUG, HOLE, 3/8", BLK	4	1U CHAS (12B & SDP40 ONLY)
21.	541-13631	FOOT, 2.00 DIA X .5H, ALUM, BLK	4	CHASSIS (MC12 ONLY)
22.				
23.	635-13637	SPCR, M3X34MM, M/F, 6MM HEX	3	ANLG TO MAIN BD
24.	635-14779	SPCR, M3X14MM, 6MM HEX	1	MEM BD TO CHASSIS
25.				
26.	640-02377	SCRW, 4-40X1/4, PNH, PH	3	MAIN BD TO REAR PNL (1) OPTO BD TO MAIN BD (2)
27.	640-13622	SCRW, 6-32X1/4, HWH, SL	2	PWR SUPPLY TO PS SPRT
28.	640-10467	SCRW, M3X6MM, FH, PH	5	PS SPRT TO CHAS (2) MEM BD TO CHAS (1) PWR SW TO PS SPRT (2)
29.	640-13645	SCRW, M4X10MM, FH, SCKT	12	COVER TO CHASSIS
30.	640-10496	SCRW, M4X10MM, PNH, PH	13	FP TO CHAS (2), FEET TO CHAS (4, MC12) MC-12B FRT TO 1U CHAS (3, 12B & SDP40) 1U CHAS TO CHAS (4, 12B & SDP40)
31.	640-10498	SCRW, M3X6MM, PNH, PH	31	VIDEO ASSY TO REAR PNL (5) ANALOG BD TO REAR PNL (5) ANALOG BD TO MAIN BD (3) MAIN BD TO CHASSIS (7) FRONT PANEL TO CHASSIS (3) PS SPRT TO CHASSIS (3) OPTION PANEL TO REAR (2) MEM BD TO CHASSIS (1) XLR BD TO 1U CHASSIS (2, 12B & SDP40)
32.	640-12534	SCRW, M3X20MM, PNH, PH	4	FAN TO PS SPRT
33.	641-01703	SCRW, TAP, AB, #4X1/4, PNH, PH	2	ACCESS PNL TO CHASSIS BOTTOM (MC12 ONLY)
34.	641-10989	SCRW, TAP, AB, #4X3/8, PNH, PH	6	REAR PNL TO CHASSIS
35.	641-11466	SCRW, TAP, #4X3/8, PNH, PH, TRI	5	RCA & OPTO CONN TO REAR PNL
36.	641-14672	SCRW, TAP, M2.5 X 8MM, PNH, PH, TRI	2	XLR CONN TO REAR PNL
37.	641-14776	SCRW, TAP, #4X3/8, FH, PH, TRI	28	XLR CONN TO 1U CHASSIS (12B & SDP40)
38.	643-10492	NUT, M4X.7MM, KEP	1	CHASSIS GND
39.	644-10494	WSHR, FL, M4 CL X 9 OD X .8MM THK	1	CHASSIS GND
40.	644-01740	WSHR, LOCK, SPLIT, #6	2	PWR SUPPLY TO PS SPRT
41.				
42.	680-11461	WIRE, 18G, G/Y, 2.5", .187 QDC/LUG #8	1	AC CONN TO CHASSIS GND
43.	680-14854	CABLE, .079, SCKT/SCKT, 4C, 4"	REF	STANDBY BD TO MAIN BD
44.	680-14081	CABLE, .100, PLUG/SCKT, 2X5C, 12"L	REF	OPTO/MIC BD TO ANLG BD
45.	680-14170	CABLE, RIB, 24-26AWG, 6CX.1, 3"	REF	OPTO/MIC BD TO MAIN BD
46.	680-14494	CABLE, .100, SCKTX2 -180, 2X17C, 6"L	1	ANLG BD TO XLR BD (12B & SDP40)
47.	680-14536	CABLE, PWR, .187/.110 QDC, SLV, 4.5"	1	AC CONN TO PWR SW
48.	680-14537	CABLE, PWR, HSG/.110 QDC, 2C, 5"	1	PWR SW TO PWR SUP
49.	680-14538	CABLE, HSG/HSG, 10C, SLV, 16/13	1	PWR SUP TO MAIN & ANLG BDS
50.	680-14539	CABLE, HSG/HSG, 4C, 4"	1	ANLG BD TO VIDEO BD

ITEM#	PART#	DESCRIPTION	QTY	WHERE USED
51.	700-14084	CHASSIS, 3U	1	
52.	700-14085	COVER, 3U	1	
53.	700-14086	SUPPORT, PS	1	
54.	700-14677	CHASSIS, IU	1	12B & SDP40 ONLY
55.	702-14094 702-14943	PANEL, REAR, MC12/B PANEL, REAR, SDP40	1	
56.	702-14097	PANEL, OPTION, BLANK	1	REAR PANEL
57.	702-14495	PANEL, ACCESS	1	CHASSIS BOTTOM (MC12 ONLY)
58.	702-14454	PANEL, FRONT, 1U	1	12B & SDP40 ONLY
59.	720-14749	TAPE, FOAM, SGL-STK, 1/4TH X 1" W	3"	ANLG SHIELD
60.	720-13632	PAD, FOOT, 1.5 DIA	4	FOOT (MC12) 1U CHAS (12B & SDP40)
61.	720-14852	GASKET, FAN	1	FAN TO PS SUPPORT
62.	740-08556	LABEL, GROUND SYMBOL, 0.5" DIA	1	PS SUPPORT
63.				
64.	740-09538	LABEL, S/N, CHASSIS	1	REAR PANEL
65.	740-14888	LABEL, DOLBY/THX/EX/DTS-ES/WARN	1	CHASSIS BOTTOM
66.	740-14798	LABEL, FUSE, CAUTION, F1	1	PS SUPPORT
67.				
68.	750-14532	PWR SUP, +-5V/+-15V, 90W	1	
69.				
70.	680-12320	CABLE, .100, PLUG/SCKT, 2X30C, 1.5"L	REF	ANLG BD TO MAIN BD
71.	680-14083	CABLE, .100, PLUG/SCKT, 2X13C, 2"L	REF	SW/LED BD TO MAIN BD
72.	680-14855	CABLE, .100, PLUG/SCKT, 2X7C, 6"L	REF	VIDEO BD TO MAIN BD
73.				
74.	630-15011	SPCR, #6CLX3/16, 1/4RD, NYL	2	ANLG SHLD TO ANLG BD
75.	640-10495	SCRW, M3X12MM, PNH, PH	2	ANLG SHLD TO ANLG BD
76.	643-10491	NUT, M3X.5MM, KEP	2	ANLG SHLD TO ANLG BD
77.	701-15010	SHIELD, ANLG BD		
78.	510-14993	CONN, POST, .200, .045, HDR	REF	MAIN BD J5 (SDP40 ONLY)
79.	680-14994	CABLE, HSG/DIN, 5C, 6"	1	REAR PNL TO MAIN BD (SDP40 ONLY)
80.	640-06517	SCRW, M2.5X4MM, PNH, PH, ZN	2	DIN CABLE TO REAR PNL (SDP40)

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	NEW LABEL ITEM 65 PER DCR #010413-00	AN 4/17/01 RL 4/25/01 WH 4/25/01	CW 4/26/01 KB 4/26/01
2	ADD ITEMS 74-77 PER ECO #010605-00	AN 6/7/01 RL 6/11/01 WH 6/11/01	CW 6/11/01 KB 6/11/01
3	ADD SDP-40 PER DCR #010508-00 ADD TAPE (ITEM 59) PER ECO #010723-00	AN 7/24/01 RL 7/24/01 WH 7/24/01	CW 8/17/01 KB 8/20/01

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE THE BOMS:
   #022-14060 CHASSIS ASSY, COMMON
   #022-14072 POWER SUPPLY ASSY
   #022-14076 MC-12
   #022-14077 MC-12B
   #022-14985 SDP-40

NEXT ASSY	USED ON
	SDP-40
	MC-12/B
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2000 FILE NAME 14530-33

APPROVALS		DATE
DRAWN	AN	4/5/01
CHECKED	RL,WH	4/5/01
Q.C.	CW	4/6/01
ISSUED	KB	4/6/01

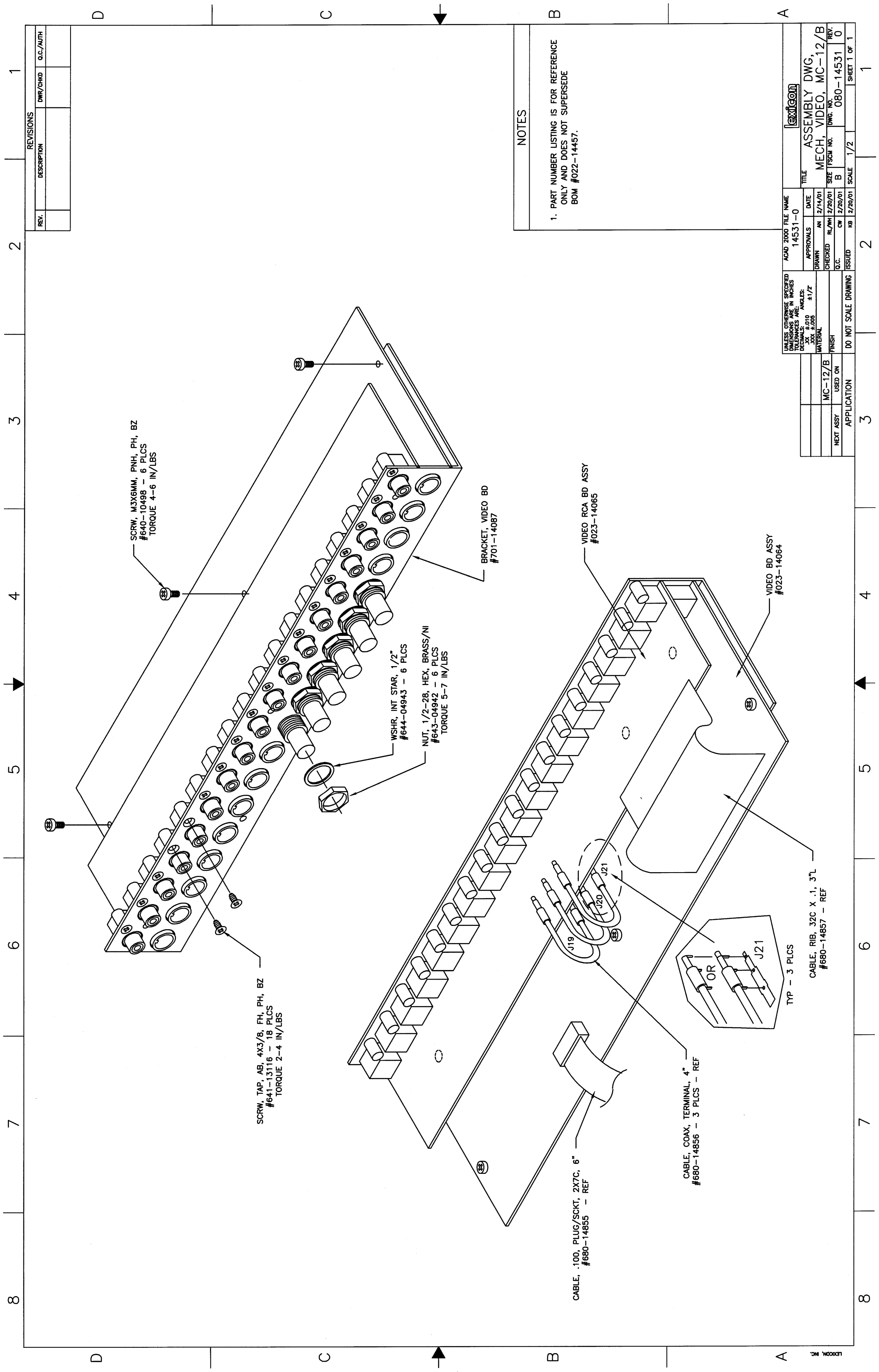
lexicon

TITLE: ASSY DWG, CHASSIS MC-12/B, SDP-40

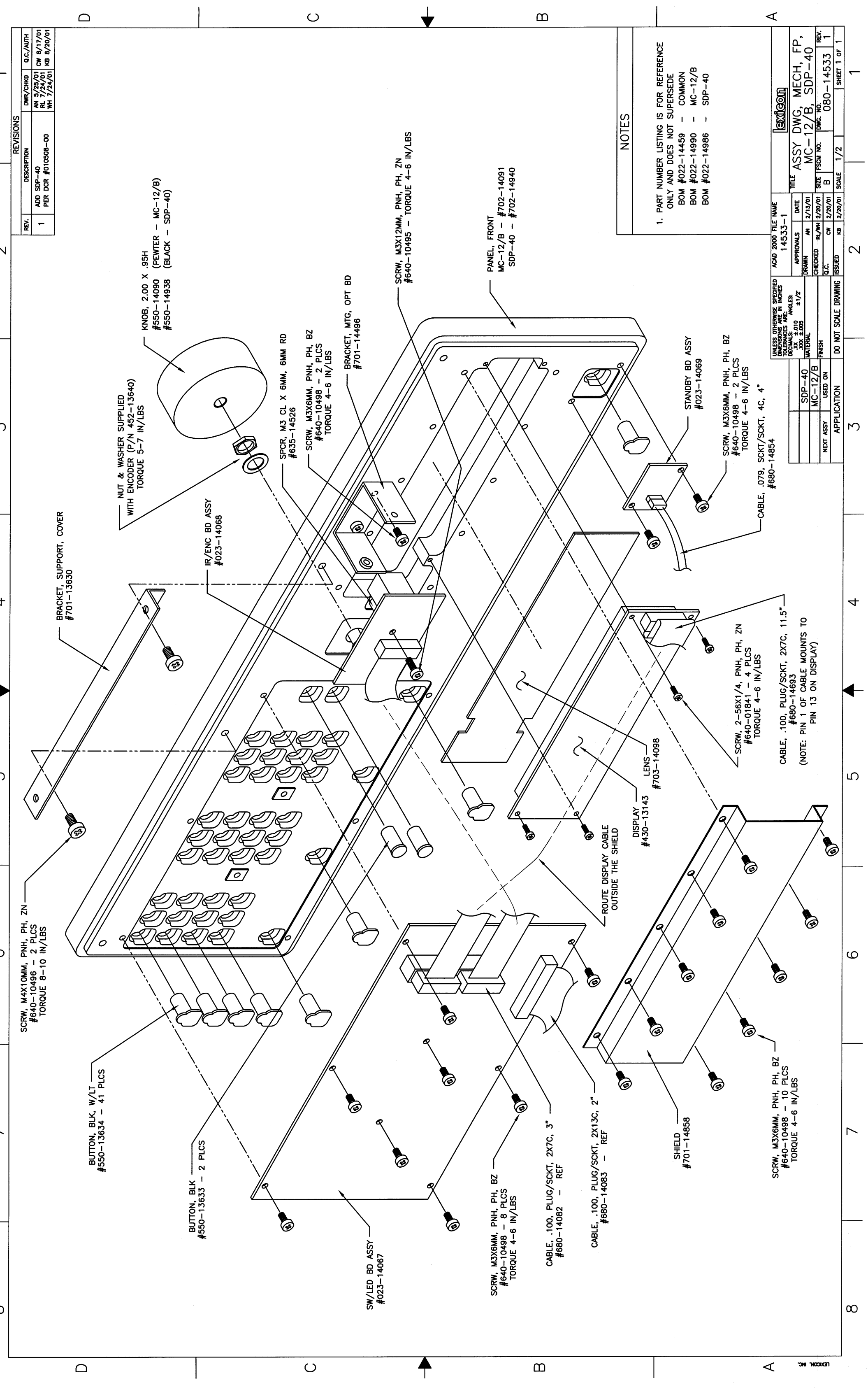
SIZE: B | FSCM NO. | DWG. NO. 080-14530 | REV. 3

SCALE: NONE | SHEET 3 OF 3

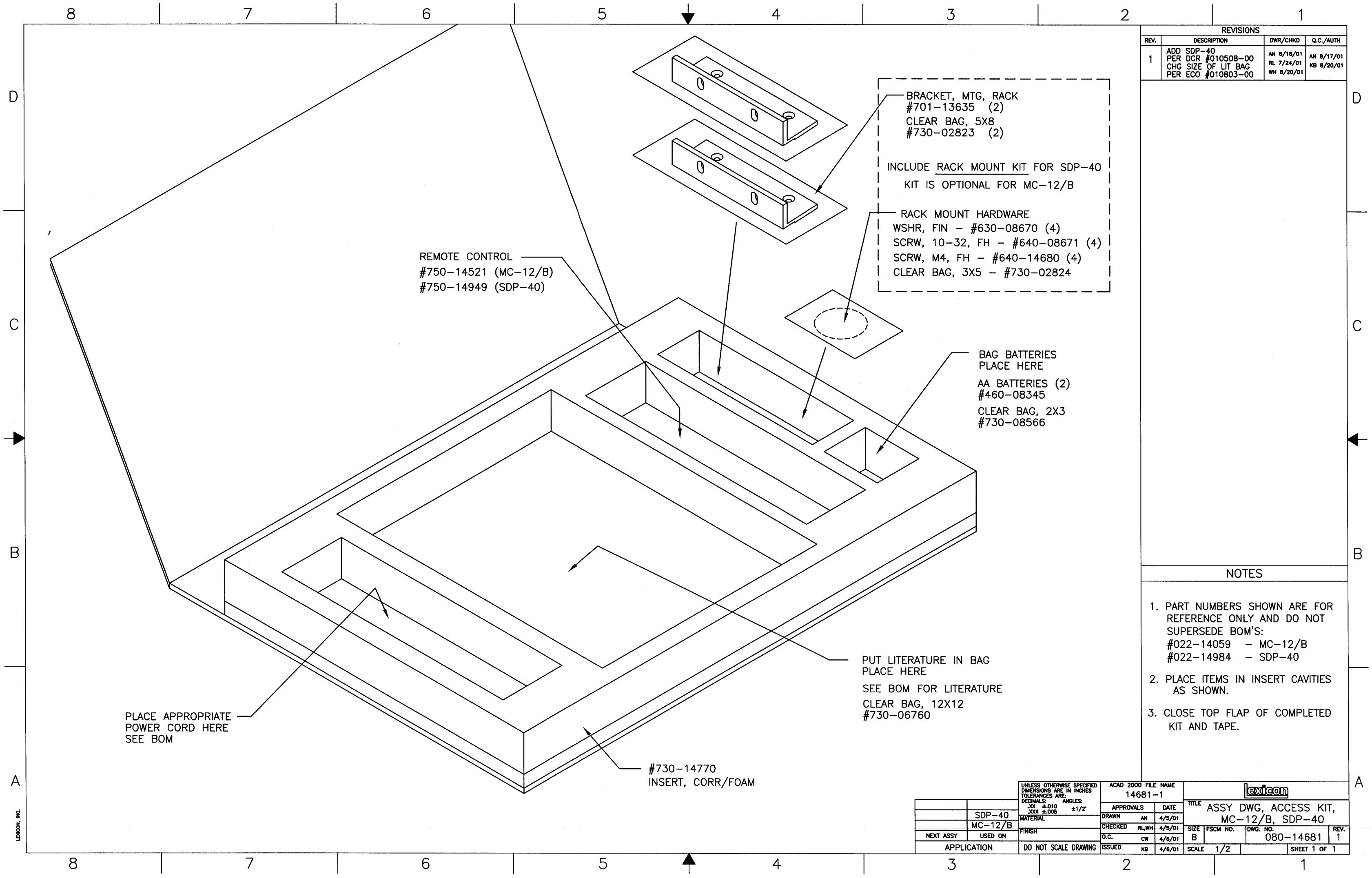
Your Notes:


REVISIONS
REV.
DESCRIPTION
DWR/CHKD
Q.C./AUTH
NOTES
1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE BOM #022-14457.
SCRW, M3X6MM, PNH, PH, BZ
#640-10498 - 6 PLCS
TORQUE 4-6 IN/LBS
BRACKET, VIDEO BD
#701-14087
WSHR, INT STAR, 1/2"
#644-04943 - 6 PLCS
NUT, 1/2-28, HEX, BRASS/NI
#643-04942 - 6 PLCS
TORQUE 5-7 IN/LBS
SCRW, TAP, AB, 4X3/8, FH, PH, BZ
#641-13116 - 18 PLCS
TORQUE 2-4 IN/LBS
VIDEO RCA BD ASSY
#023-14065
VIDEO BD ASSY
#023-14064
J19
J20
J21
OR
TYP - 3 PLCS
CABLE, RIB, 32C X .1, 3"L
#680-14857 - REF
CABLE, COAX, TERMINAL, 4"
#680-14856 - 3 PLCS - REF
CABLE, .100, PLUG/SCKT, 2X7C, 6"
#680-14855 - REF
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE: DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
NEXT ASSY
USED ON
MC-12/B
APPLICATION
DO NOT SCALE DRAWING
ACAD 2000 FILE NAME
14531-0
APPROVALS
DATE
DRAWN AN 2/14/01
CHECKED RL/WH 2/20/01
Q.C. CW 2/20/01
ISSUED KB 2/20/01
lexicon
TITLE
ASSEMBLY DWG, MECH, VIDEO, MC-12/B
SIZE B
FSCM NO.
DWG. NO. 080-14531
REV. 0
SCALE 1/2
SHEET 1 OF 1
LEXICON, INC.

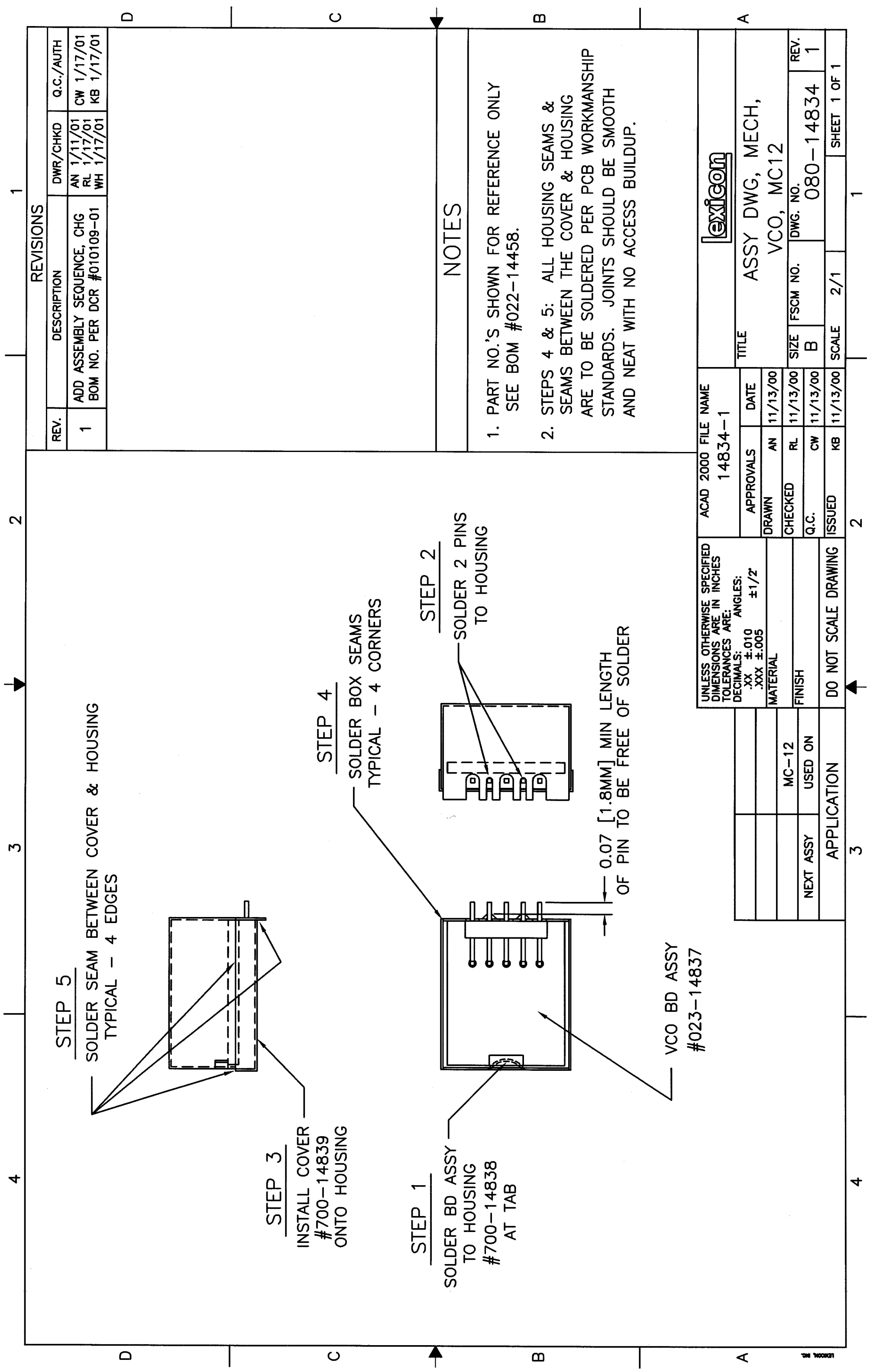
Your Notes:


REVISIONS
REV. DESCRIPTION DWR/CHKD Q.C./AUTH
1 ADD SDP-40 PER DCR #010508-00
KNOB, 2.00 X 95H
#550-14090 (PEWTER - MC-12/B)
#550-14938 (BLACK - SDP-40)
NUT & WASHER SUPPLIED WITH ENCODER (P/N 452-13640) TORQUE 5-7 IN/LBS
SPCR, M3 CL X 6MM, 6MM RD #635-14526
SCRW, M3X6MM, PNH, PH, BZ #640-10498 - 2 PLCS TORQUE 4-6 IN/LBS
BRACKET, MTG, OPT BD #701-14496
SCRW, M3X12MM, PNH, PH, ZN #640-10495 - TORQUE 4-6 IN/LBS
PANEL, FRONT MC-12/B - #702-14091 SDP-40 - #702-14940
NOTES
1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE
BOM #022-14459 - COMMON
BOM #022-14990 - MC-12/B
BOM #022-14986 - SDP-40
STANDBY BD ASSY #023-14069
SCRW, M3X6MM, PNH, PH, BZ #640-10498 - 2 PLCS TORQUE 4-6 IN/LBS
CABLE, .079, SCKT/SCKT, 4C, 4" #680-14854
BRACKET, SUPPORT, COVER #701-13630
IR/ENC BD ASSY #023-14068
SCRW, 2-56X1/4, PNH, PH, ZN #640-01841 - 4 PLCS TORQUE 4-6 IN/LBS
CABLE, .100, PLUG/SCKT, 2X7C, 11.5" #680-14693 (NOTE: PIN 1 OF CABLE MOUNTS TO PIN 13 ON DISPLAY)
LENS #703-14098
DISPLAY #430-13143
ROUTE DISPLAY CABLE OUTSIDE THE SHIELD
SCRW, M4X10MM, PNH, PH, ZN #640-10496 - 2 PLCS TORQUE 8-10 IN/LBS
BUTTON, BLK, W/LT #550-13634 - 41 PLCS
BUTTON, BLK #550-13633 - 2 PLCS
SW/LED BD ASSY #023-14067
SCRW, M3X6MM, PNH, PH, BZ #640-10498 - 8 PLCS TORQUE 4-6 IN/LBS
CABLE, .100, PLUG/SCKT, 2X7C, 3" #680-14082 - REF
CABLE, .100, PLUG/SCKT, 2X13C, 2" #680-14083 - REF
SHIELD #701-14858
SCRW, M3X6MM, PNH, PH, BZ #640-10498 - 10 PLCS TORQUE 4-6 IN/LBS
ACAD 2000 FILE NAME 14533-1
ASSY DWG, MECH, FP, MC-12/B, SDP-40
DWG. NO. 080-14533
REV. 1
SHEET 1 OF 1
SCALE 1/2
SDP-40
MC-12/B
NEXT ASSY USED ON
APPLICATION
DO NOT SCALE DRAWING

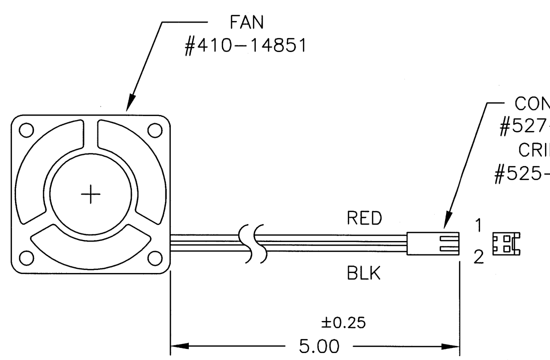
Your Notes:


REVISIONS
REV. | DESCRIPTION | DWR/CHKD | Q.C./AUTH
1 | ADD SDP-40 PER DCR #010508-00 CHG SIZE OF LIT BAG PER ECO #010803-00 | AN 6/18/01 RL 7/24/01 WH 8/20/01 | AN 8/17/01 KB 8/20/01
BRACKET, MTG, RACK
#701-13635 (2)
CLEAR BAG, 5X8
#730-02823 (2)
INCLUDE RACK MOUNT KIT FOR SDP-40
KIT IS OPTIONAL FOR MC-12/B
RACK MOUNT HARDWARE
WSHR, FIN - #630-08670 (4)
SCRW, 10-32, FH - #640-08671 (4)
SCRW, M4, FH - #640-14680 (4)
CLEAR BAG, 3X5 - #730-02824
REMOTE CONTROL
#750-14521 (MC-12/B)
#750-14949 (SDP-40)
BAG BATTERIES
PLACE HERE
AA BATTERIES (2)
#460-08345
CLEAR BAG, 2X3
#730-08566
PUT LITERATURE IN BAG
PLACE HERE
SEE BOM FOR LITERATURE
CLEAR BAG, 12X12
#730-06760
PLACE APPROPRIATE
POWER CORD HERE
SEE BOM
#730-14770
INSERT, CORR/FOAM
NOTES
1. PART NUMBERS SHOWN ARE FOR REFERENCE ONLY AND DO NOT SUPERSEDE BOM'S:
#022-14059 - MC-12/B
#022-14984 - SDP-40
2. PLACE ITEMS IN INSERT CAVITIES AS SHOWN.
3. CLOSE TOP FLAP OF COMPLETED KIT AND TAPE.
SDP-40
MC-12/B
NEXT ASSY
USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005
ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING
ACAD 2000 FILE NAME
14681-1
APPROVALS | DATE
DRAWN AN 4/5/01
CHECKED RL,WH 4/5/01
Q.C. CW 4/6/01
ISSUED KB 4/6/01
lexicon
TITLE ASSY DWG, ACCESS KIT, MC-12/B, SDP-40
SIZE B
FSCM NO.
DWG. NO. 080-14681
REV. 1
SCALE 1/2
SHEET 1 OF 1

Your Notes:


REVISIONS
REV.
DESCRIPTION
DWR/CHKD
Q.C./AUTH
1
ADD ASSEMBLY SEQUENCE, CHG BOM NO. PER DCR #010109-01
AN 1/11/01 RL 1/17/01 WH 1/17/01
CW 1/17/01 KB 1/17/01
NOTES
1. PART NO.'S SHOWN FOR REFERENCE ONLY SEE BOM #022-14458.
2. STEPS 4 & 5: ALL HOUSING SEAMS & SEAMS BETWEEN THE COVER & HOUSING ARE TO BE SOLDERED PER PCB WORKMANSHIP STANDARDS. JOINTS SHOULD BE SMOOTH AND NEAT WITH NO ACCESS BUILDUP.
STEP 5
SOLDER SEAM BETWEEN COVER & HOUSING TYPICAL - 4 EDGES
STEP 4
SOLDER BOX SEAMS TYPICAL - 4 CORNERS
STEP 2
SOLDER 2 PINS TO HOUSING
STEP 3
INSTALL COVER #700-14839 ONTO HOUSING
STEP 1
SOLDER BD ASSY TO HOUSING #700-14838 AT TAB
0.07 [1.8MM] MIN LENGTH OF PIN TO BE FREE OF SOLDER
VCO BD ASSY #023-14837
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING
ACAD 2000 FILE NAME
14834-1
APPROVALS
DATE
DRAWN AN 11/13/00
CHECKED RL 11/13/00
Q.C. CW 11/13/00
ISSUED KB 11/13/00
MC-12
NEXT ASSY
USED ON
APPLICATION
lexicon
TITLE
ASSY DWG, MECH, VCO, MC12
SIZE B
FSCM NO.
DWG. NO. 080-14834
REV. 1
SCALE 2/1
SHEET 1 OF 1

Your Notes:



NOTE:

LEXICON P/N'S 527-12537 & 525-12536 REFER TO AMP P/N'S. EQUIVALENT PARTS FROM OTHER VENDORS ARE ALLOWED, PROVIDED BOTH THE HOUSING & THE CONTACT ARE MADE BY THE SAME VENDOR.

REVISIONS

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ALLOW ALTERNATE VENDORS FOR CONN HOUSING & CONTACTS PER DCR #010409-00	AN 4/16/01 RL 4/16/01 WH 4/16/01	CW 4/18/01 KB 4/18/01

NOTES

1. SEE BOM #022-14850

	MC-12
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD 2000 FILE NAME 14853-1

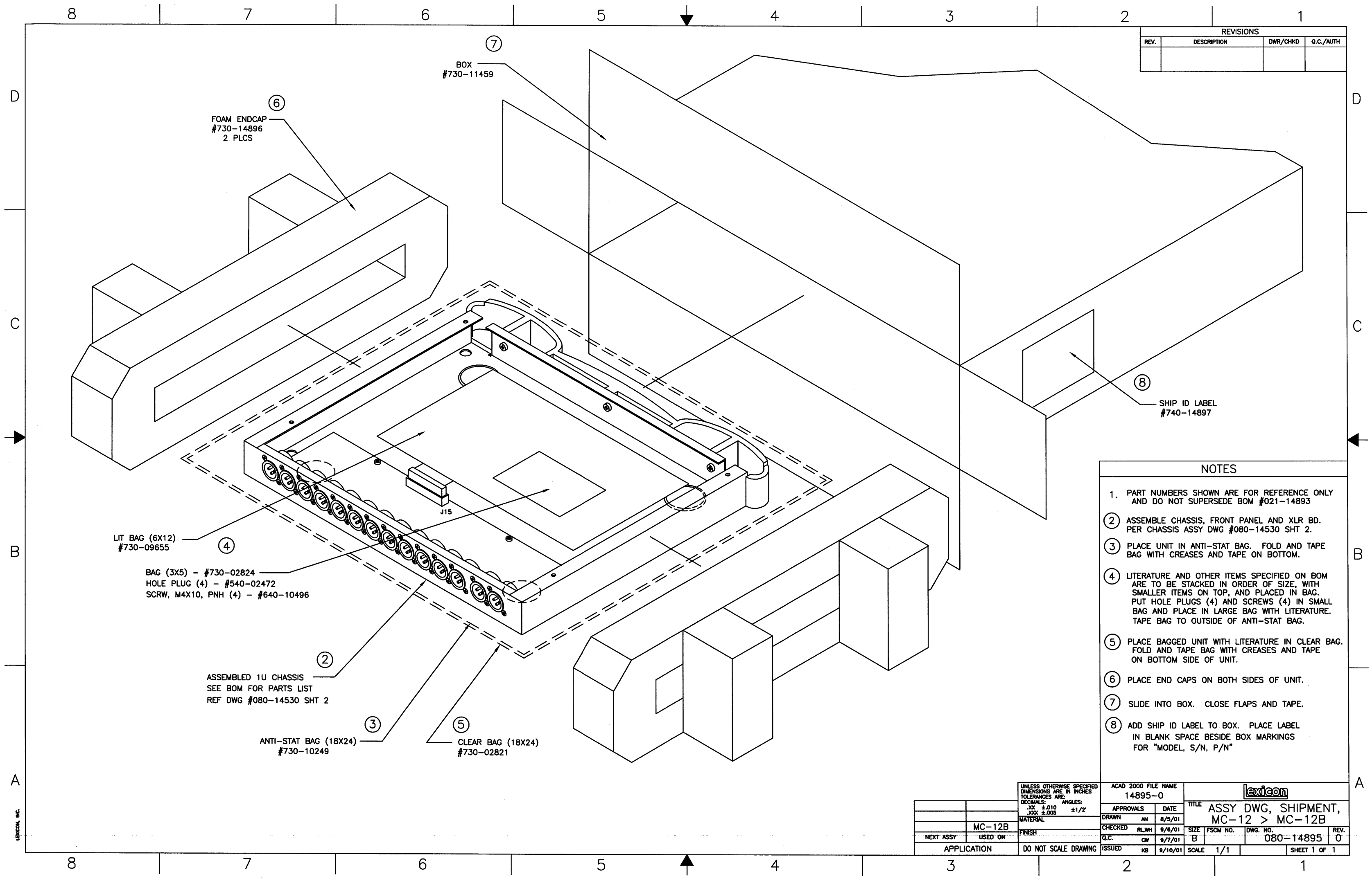
APPROVALS		DATE
DRAWN	AN	1/16/01
CHECKED	RL WH	1/19/01 1/22/01
Q.C.	CW	1/22/01
ISSUED	KB	1/22/01

lexicon

TITLE ASSY DWG, FAN, MC-12

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-14853	1
SCALE N/A		SHEET 1 OF 1	

Your Notes:


BOX
#730-11459
FOAM ENDCAP
#730-14896
2 PLCS
SHIP ID LABEL
#740-14897
LIT BAG (6X12)
#730-09655
BAG (3X5) - #730-02824
HOLE PLUG (4) - #540-02472
SCRW, M4X10, PNH (4) - #640-10496
J15
ASSEMBLED 1U CHASSIS
SEE BOM FOR PARTS LIST
REF DWG #080-14530 SHT 2
ANTI-STAT BAG (18X24)
#730-10249
CLEAR BAG (18X24)
#730-02821
REVISIONS
REV. DESCRIPTION DWR/CHKD Q.C./AUTH
NOTES
1. PART NUMBERS SHOWN ARE FOR REFERENCE ONLY AND DO NOT SUPERSEDE BOM #021-14893
2 ASSEMBLE CHASSIS, FRONT PANEL AND XLR BD. PER CHASSIS ASSY DWG #080-14530 SHT 2.
3 PLACE UNIT IN ANTI-STAT BAG. FOLD AND TAPE BAG WITH CREASES AND TAPE ON BOTTOM.
4 LITERATURE AND OTHER ITEMS SPECIFIED ON BOM ARE TO BE STACKED IN ORDER OF SIZE, WITH SMALLER ITEMS ON TOP, AND PLACED IN BAG. PUT HOLE PLUGS (4) AND SCREWS (4) IN SMALL BAG AND PLACE IN LARGE BAG WITH LITERATURE. TAPE BAG TO OUTSIDE OF ANTI-STAT BAG.
5 PLACE BAGGED UNIT WITH LITERATURE IN CLEAR BAG. FOLD AND TAPE BAG WITH CREASES AND TAPE ON BOTTOM SIDE OF UNIT.
6 PLACE END CAPS ON BOTH SIDES OF UNIT.
7 SLIDE INTO BOX. CLOSE FLAPS AND TAPE.
8 ADD SHIP ID LABEL TO BOX. PLACE LABEL IN BLANK SPACE BESIDE BOX MARKINGS FOR "MODEL, S/N, P/N"
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING
MC-12B
NEXT ASSY USED ON
APPLICATION
ACAD 2000 FILE NAME 14895-0
APPROVALS DATE
DRAWN AN 8/5/01
CHECKED RL,WH 9/6/01
Q.C. CW 9/7/01
ISSUED KB 9/10/01
lexicon
TITLE ASSY DWG, SHIPMENT, MC-12 > MC-12B
SIZE B FSCM NO. DWG. NO. 080-14895 REV. 0
SCALE 1/1 SHEET 1 OF 1
LEXICON, INC.

Lexicon, Inc.
3 Oak Park
Bedford, MA 01730-1441
Tel: 781-280-0300
Customer Service Fax: 781-280-0499
Email: csupport@lexicon.com
www.lexicon.com

Lexicon Part No. 070-14828 Rev 0 Printed in U.S.A.